

關鍵字:

Ken Modified 07/21_**A00
Ken Modified 08/11_**A00
Ken Modified 08/13_**A00
Ken Modified 08/14_**A00
Ken Modified 08/17_**A00
Ken Modified 08/19_**A00

Blackwell-T4 8" Schematic
Cherry Trail - T4
2015-08-20
REV : A00

BOM 修改:

Snowfield : WU3701:054.03096.0001
Charger Mosfet (BOM變更)
Old P/N:ZZ.00215.037 Location: PU4603
New P/N: 84.03664.037 Location: PU4603
Second P/N:84.00920.037
TPS65982:65982074.65982.007Z ->074.65982.0B7Z
CPU:071.CHERY.0D0U->57VYD

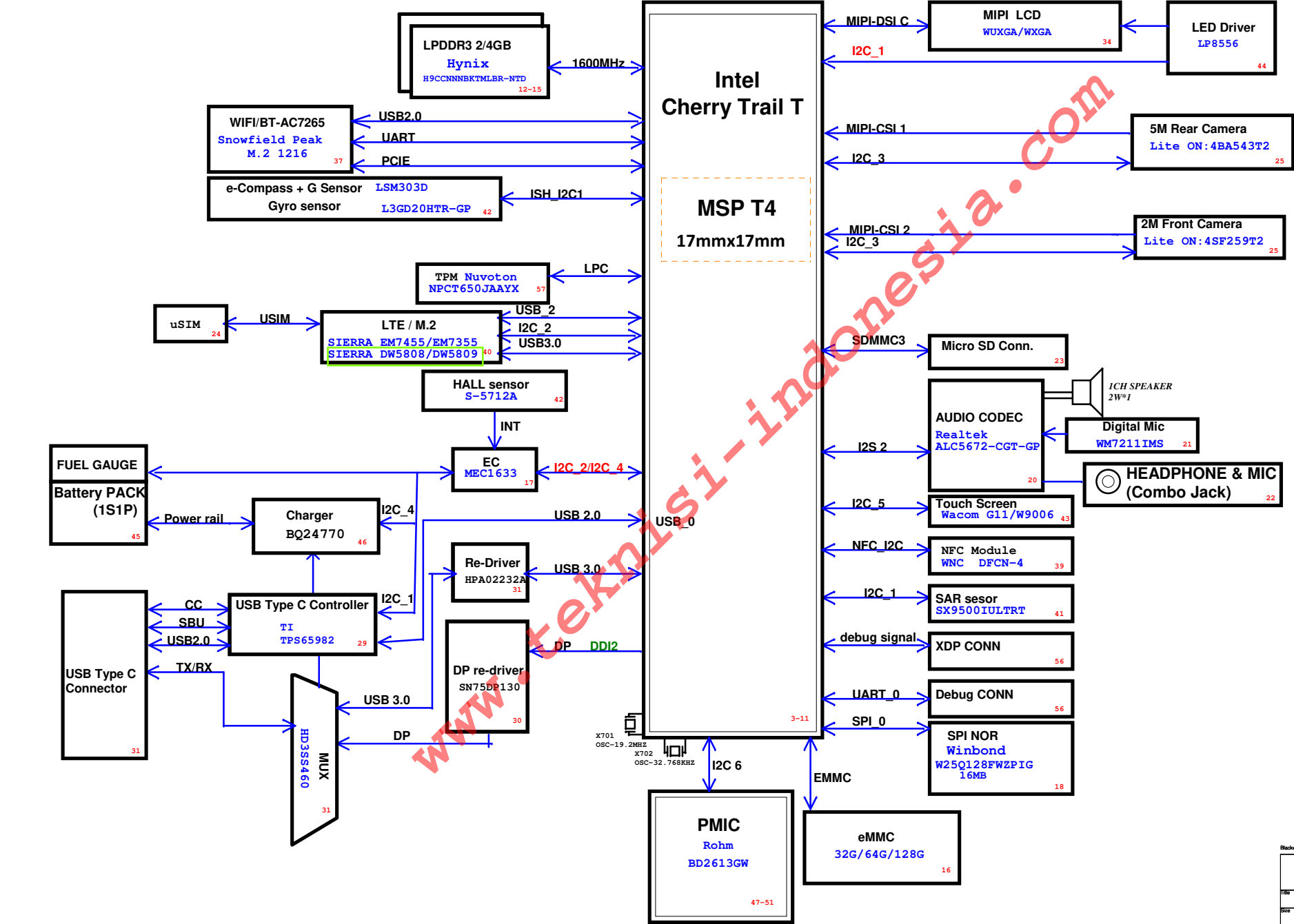
EC U1704 量產料號更改為:071.01633.0A0U
Cap 更改料號 78.10612.5BL->078.10612.05BN
Audio Codec U2001:071.03272.0003
Cancel XDP1,DB2,R735,R736,R740,R751
CAP更改料號 78.2R2B2.1SLRL -> 78.2R2B2.1SL
78.68034.1FLLL -> 78.68034.1FL

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<Core Design>

| | | | |
|----------------------------------|-----------------|--|-----|
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| Title 01_Cover | | | |
| Size | Document Number | | Rev |
| | Blackwell T4 | | -1 |
| Date: Thursday, October 01, 2015 | | Sheet 1 of | 73 |

Block Diagram

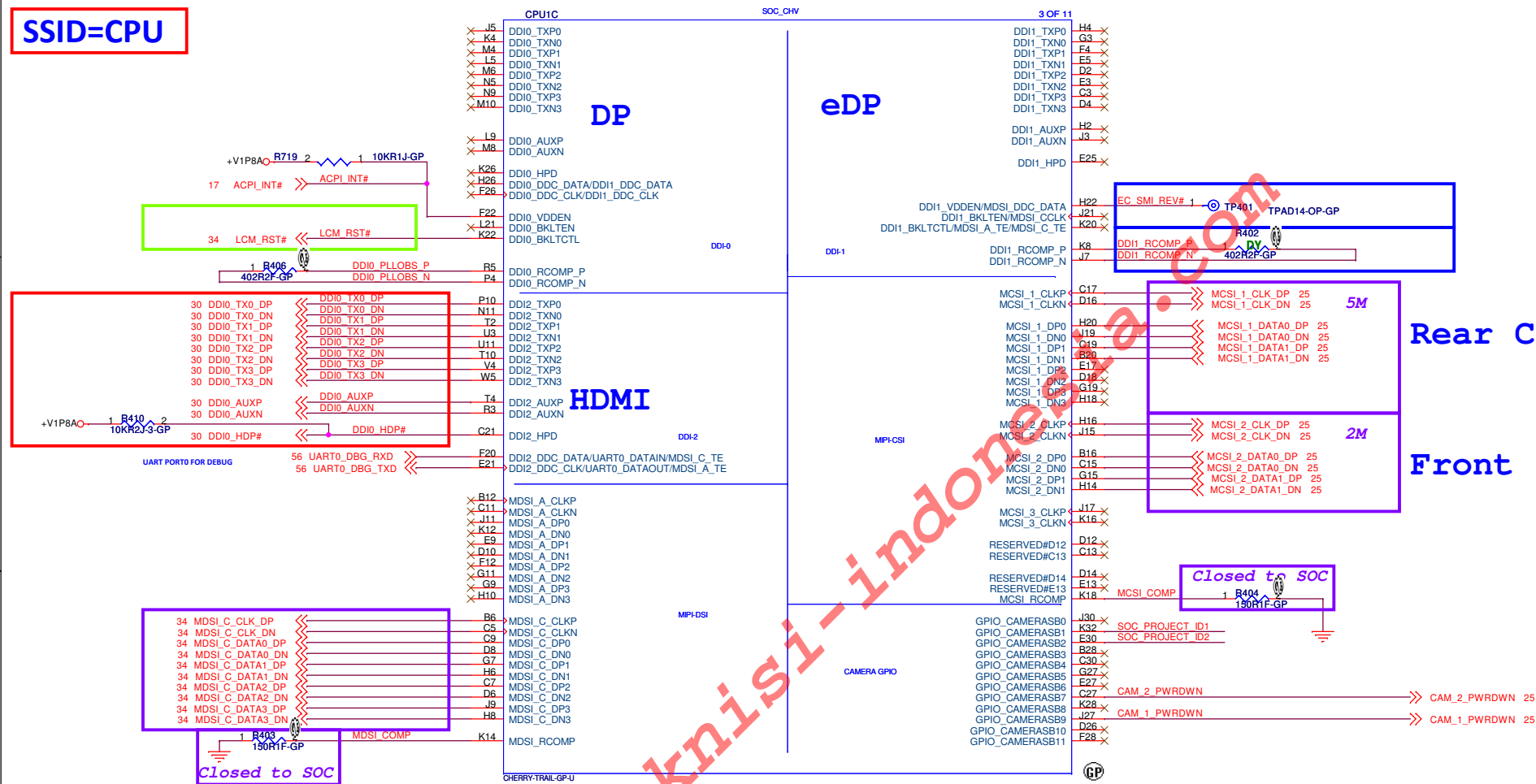


SSID=CPU

Sheet 3 of 73

SOC : DDI 0&1 / MIPI-DIS/MIPI-CSI/MIPI-GPIO

SSID=CPU

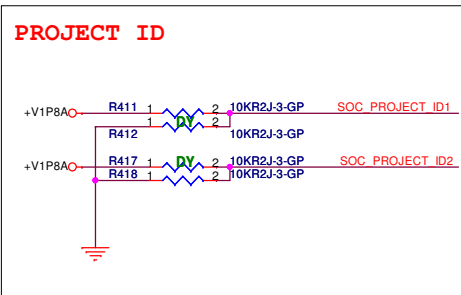


Rear Camera

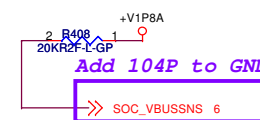
Front Camera

Closed to SOC

Closed to SOC



| SOC PROJECT ID | | |
|----------------|-------------|-------------|
| PROJECT | PROJECT_ID2 | PROJECT_ID1 |
| Blackwell-T3 | 0 | 0 |
| Blackwell-T4 | 0 | 1 |
| Somerset-T3 | 1 | 0 |
| Somerset-T4 | 1 | 1 |

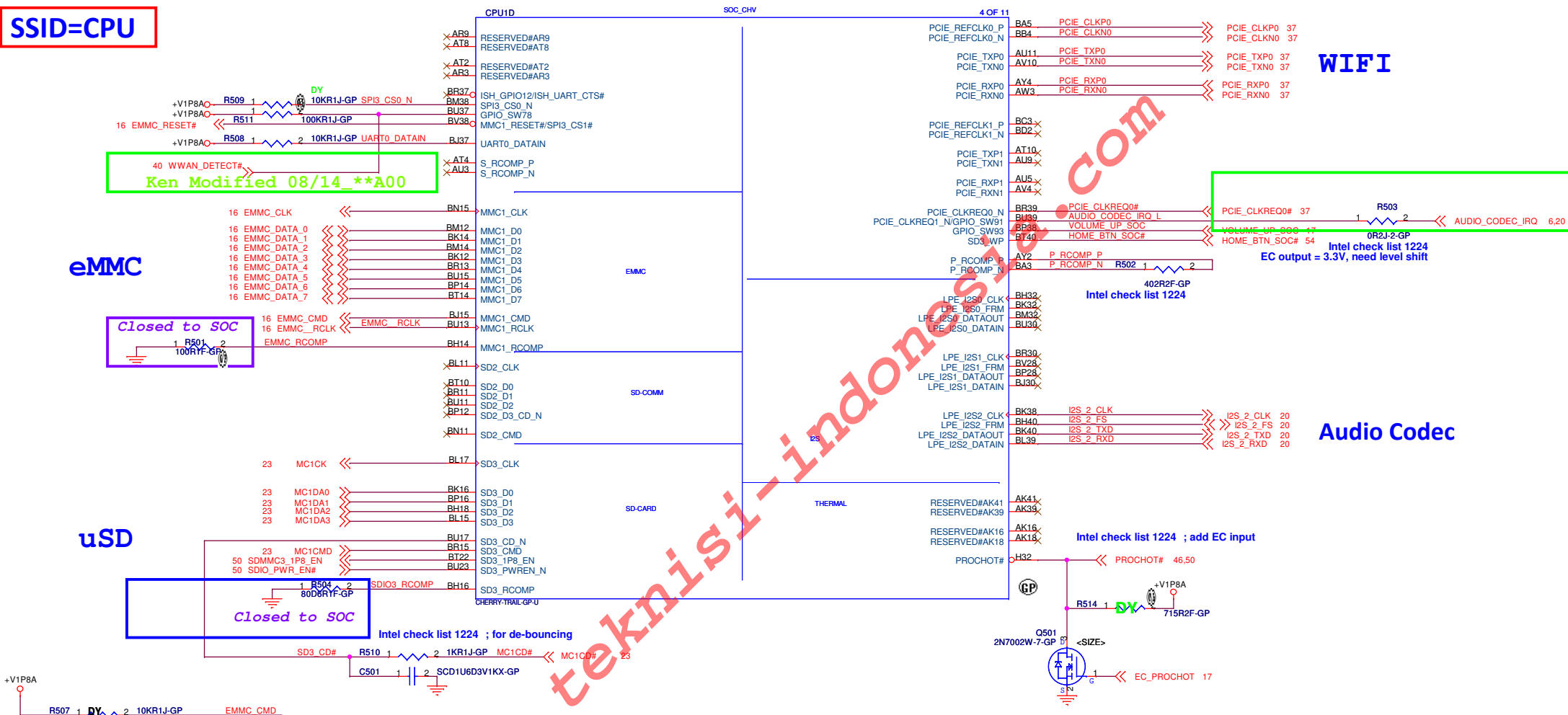


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| Blackwell T4 | |
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: 04_SOC (eDP/HDMI/MIPI) | |
| Size: Document Number | Rev: -1 |
| Date: Thursday, October 01, 2015 | Sheet: 4 of 73 |

SOC : eMMC/SD/GPIO/I2S

SSID=CPU

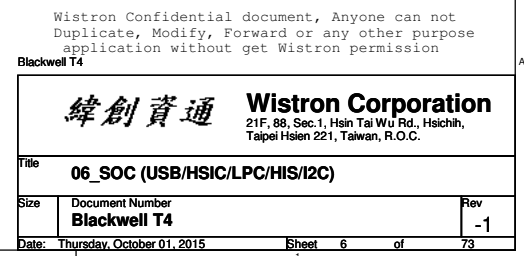


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| Title 05_SOC (EMMC/SD/GPIO/I2S) | |
| Size Document Number Blackwell T4 | Rev -1 |
| Date: Thursday, October 01, 2015 | Sheet 5 of 73 |

SSID=CPU



SSID=CPU

| | | | | | | |
|------------------|--------|----------------|-----------------|--------------|---|------------|
| 25 PLT_CLK1_CAM1 | R723_1 | 2P2R2-2-GP | PLT_CLK1_CAM1_1 | B8B | PMC_PLT_CLK0/ISH_GPIO10/ISH_UART_DATAIN | PLT CLOCK |
| 55 PLT_CLK1_CAM2 | R722_1 | | PLT_CLK1_CAM2_1 | B8A | PMC_PLT_CLK1/ISH_GPIO11/ISH_UART_DATOUT | |
| 20 CLK_I2S_MCLK | R728_1 | 2P2R2-2-GP | CLK_I2S_MCLK_1 | X-BUL | PMC_PLT_CLK2/ISH_GPIO12/ISH_UART_CTS# | TAPORTITPT |
| 56 ISH_I2C0_SDA | | | ISH_I2C0_SDA | B87 | PMC_PLT_CLK3/ISH_GPIO13/ISH_UART_RTS# | |
| 56 ISH_I2C0_SCL | | | ISH_I2C0_SCL | B1E | PMC_PLT_CLK4/ISH_GPIO14/ISH_I2C0_DATA | |
| | | | | | PMC_PLT_CLK5/ISH_GPIO15/ISH_I2C0_CLK | |
| link to XDP | | | | | | |
| | | 56 XDP_H_TCK | F34 | JTAG_TCK | | |
| | | 56 XDP_H_TRST# | E36 | JTAG_TRST# | | |
| | | 56 XDP_H_TMS | B34 | JTAG_TMS | | |
| | | 56 XDP_H_TDI | E33 | JTAG_TDI | | |
| | | 56 XDP_H_TDO | J33 | JTAG_TDO | | |
| | | 56 XDP_H_PRDY# | G33 | JTAG_PRDY# | | |
| | | 56 XDP_H_PREQ# | H34 | JTAG_PREQ# | | |
| +V1P8A | | | X-BNS | RESERVED#BN9 | | |

P8A

50

TO
110

100

NFC



—

3-GF
10 S

10 S

—

| CPUIF1 | SOC, CHV | | 6 CPU1 |
|--|---------------|---|--------|
| ICLK_OSCIN ICLK_OSCOUT RESERVED#B09 ICLK_RCOMP ICLK_ICOMP RESERVED#AY12 RESERVED#B08 RESERVED#AC28 RESERVED#AF28 RESERVED#AH27 | ICLK | HSIUART UART1_DATAOUT/UART0_DATAOUT UART1_DATAIN/UART0_DATAIN UART1_RTS# UART1_CTS# UART2_DATAOUT UART2_DATAIN UART2_RTS# UART2_CTS# | |
| | | PMU PMC_SUSPWRDNACK PMC_SUSCLK0 PMC_SLP_S0UX# PMC_SLP_S# PMC_SLP_S3# PMC_ACPRESENT PMC_BATLOW# PMC_PWRBTN# PMC_RSTBTN# PMC_PLTRST# PMC_WAKE# PMC_SUS_STAT# | |
| PMC_PLT_CLK0/ISH_GPIO10/ISH_UART_DATAOUT PMC_PLT_CLK1/ISH_GPIO11/ISH_UART_DATAIN PMC_PLT_CLK2/ISH_GPIO12/ISH_UART_CTS# PMC_PLT_CLK3/ISH_GPIO13/ISH_UART_RTS# PMC_PLT_CLK4/ISH_GPIO14/ISH_I2CO_DATA PMC_PLT_CLK5/ISH_GPIO15/ISH_I2CO_CLK | PLT_CLOCK | | |
| JTAG_TCK JTAG_TRST# JTAG_TMS JTAG_TDI JTAG_TDO JTAG_PROG# JTAG_FREQ# RESERVED#B09 | TAP PORT/TTIP | RTC RTC_TEST# RESERVED#B01 PMC_RSMRST# PMC_CORE_PWROK RTC_RST# RTC_X1 RTC_X2 RTC_EXTIPAD | |
| FST_SPL_CLK FST_SPL_D3 FST_SPL_D2 FST_SPL_D1 FST_SPL_D0 FST_SPL_CS0# FST_SPL_CS1# FST_SPL_CS2# | FAST SPI | SVID SVID_ALERT# SVID_DATA SVID_CLK PWM PWM1/ISH_GPIO10/ISH_UART_DATAOUT | |
| GPIO_SUS0 GPIO_SUS1/SEC_MSTR_TCK GPIO_SUS2/SEC_MSTR_TMS GPIO_SUS3/SEC_MSTR_TDI GPIO_SUS4/SEC_MSTR_TDO GPIO_SUS5/PMC_SUSCLK1 GPIO_SUS6/PMC_SUSCLK2 GPIO_SUS7/PMC_SUSCLK3 GPIO_SUS8 GPIO_SUS9 GPIO_SUS10 | GPIO SUS | GPIO_DFX0/CO_BPM0_TX GPIO_DFX1/CO_BPM1_TX/OT1_BPM1_TX GPIO_DFX2/CO_BPM2_TX/ISH_GPIO13 GPIO_DFX3/CO_BPM3_TX GPIO_DFX4 GPIO_DFX5/CO_BPM0_TX/CO_BPM1_TX GPIO_DFX6/CO_BPM1_TX/CO_BPM1_TX GPIO_DFX7/CO_BPM1_TX/CO_BPM1_TX GPIO_DFX8/CO_BPM3_TX/CO_BPM3_TX GPIO_ALERT1/ISH_GPIO11/ISH_UART_DATAIN GPIO_DFX GPIO10_ROMP | |
| RESERVED#B08 RESERVED#B010 RESERVED#B09 | | SPI1 SPI1_MISO SPI1_MOSI SPI1_CLK SPI1_CS0# SPI1_CS# | |

BT UART

HDMI to DP UART

Net: SUS_PWRDNACK link to PMIC
Net: SLP_S0iX_N link to XDP, Touch

Net: SLP_S3_N link to camera, PMIC

Net: AC_PRESENT link to PMIC
Net: PMU_BATTLOW_N link to PMIC
Net: SOC_PWRBTN_N link to PMIC

Net: PLTRST_N link to PMIC, XDP
Net: SOC wakeup from WIFI

PMU_SLP_S0i3_N link to XDP

SOC_RTEST_N link to PMIC and XDP

RSMRST_N link to PMIC and XDP
CORE_PWRK link to PMIC and XDP

SRT_CRST_N link to XDP

Check with Int

EC and SOC

MODEM_PWR_ON >> MODEM_PWR_C

BT_DEV_EN >> BT_DEV_EN_57

EC_SMI# >> EC_SMI# 17

COCO_ID >> COCO_ID

VOLUME_DOWN SOC << VOLUME_DOWN

RF_WWAN_DISABLE 1P8 << RF_WWAN_DISABLE

TOUCH_INT << TOUCH_INT# 43

Ken Modified 08/14_**A00

~~L19~~
~~K19~~ Ken Modified 08/14_**A00

Check with Intel

EC and SOC 做Handshaking

| | |
|-----------|----|
| ST_DEV_EN | 37 |
| EC_SMI# | 17 |

[VOLUME_DOWN_SOC](#) 17 [link to XDP](#)

100

10KR1J-GP

+V1P8A R734 1 DY 2 10KR2J-3-GP COO

0:Normal , 1:COCO

Wietrop, C.

applicat

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Title 07_SO

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| | Blackw |
| Date: | Thursday, C |

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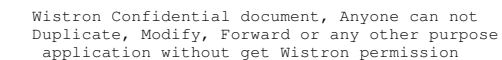
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| | | |
|-------|-------------------------------|--------------|
| Title | 07 SOC (CLK/ITP/SPI/MISC/PMU) | Blackwell T4 |
|-------|-------------------------------|--------------|

| | | | |
|------|-----------------|--------|-----|
| Size | Document Number | Custom | Rev |
|------|-----------------|--------|-----|

Date: Thursday, October 01, 2015 Sheet 7 of 73

SSID=CPU



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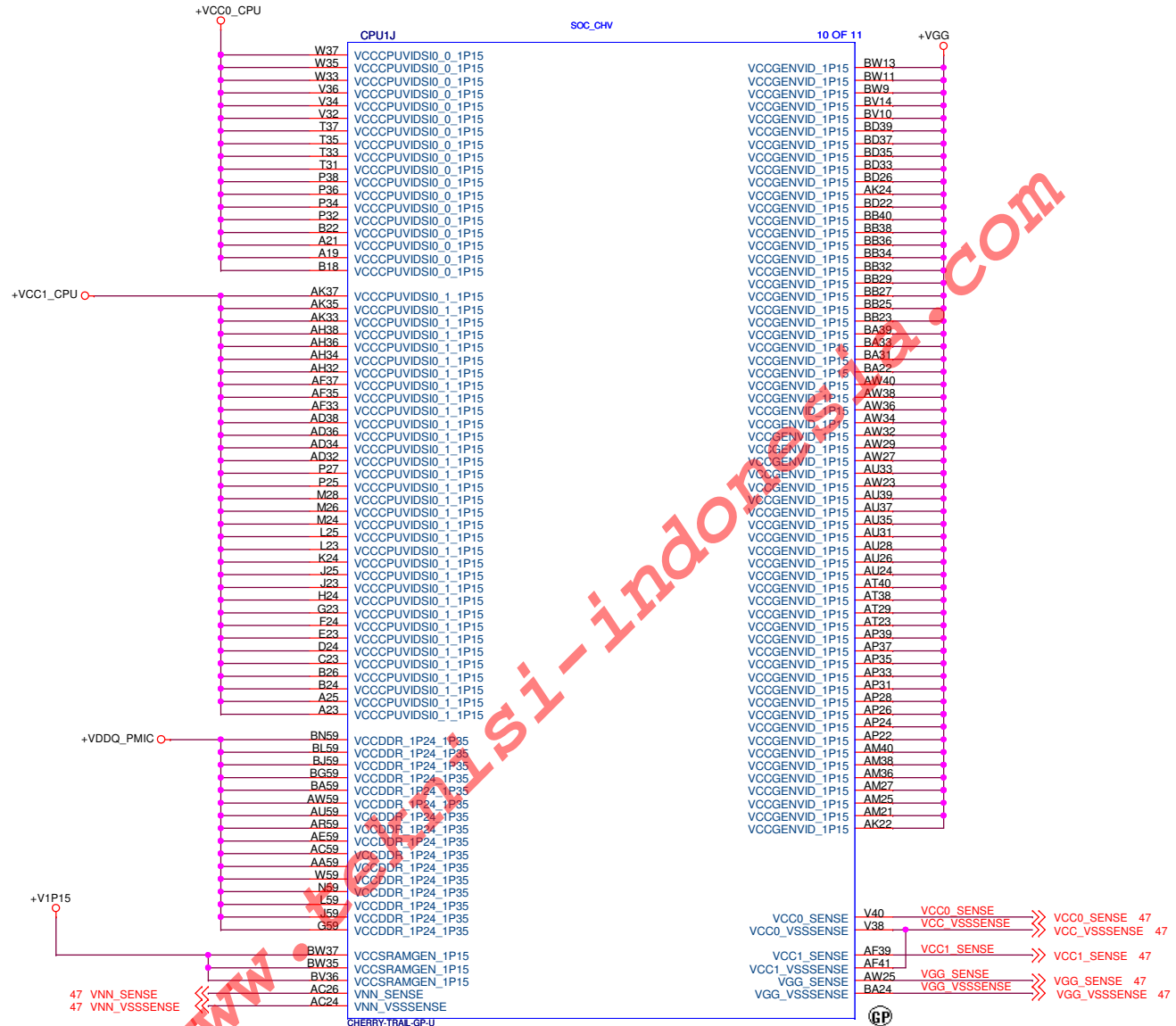
08_SOC (VCCIO)

| |
|-----|
| Rev |
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|--|----|
| | |
| | 73 |

SOC : VCC/VNN

SSID=CPU



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Title

09_SOC (VCC/VNN)

Size

Document Number

Blackwell T4

Rev

-1

Date: Thursday, October 01, 2015

Sheet 9 of 73

SOC : GROUND

SSID=CPU

| CPU1G | SOC_CHV | 7 OF 11 |
|-------|---------|---------|
| V58 | VSS | L11 |
| V54 | VSS | L7 |
| V52 | VSS | L3 |
| V46 | VSS | K58 |
| V44 | VSS | K54 |
| V42 | VSS | K50 |
| A17 | VSS | BA7 |
| AV2 | VSS | K10 |
| V29 | VSS | K6 |
| V19 | VSS | J41 |
| V17 | VSS | J13 |
| V15 | VSS | H56 |
| V8 | VSS | H46 |
| V6 | VSS | H44 |
| U59 | VSS | H40 |
| U53 | VSS | H36 |
| U51 | VSS | AM2 |
| U49 | VSS | H28 |
| U5 | VSS | H12 |
| T56 | VSS | G53 |
| T45 | VSS | G45 |
| T43 | VSS | G41 |
| T41 | VSS | D22 |
| T39 | VSS | G30 |
| T28 | VSS | G25 |
| T26 | VSS | G21 |
| T24 | VSS | G17 |
| T22 | VSS | G13 |
| T20 | VSS | G5 |
| T18 | VSS | F58 |
| T16 | VSS | F48 |
| T12 | VSS | F40 |
| T6 | VSS | BD24 |
| R59 | VSS | F18 |
| R57 | VSS | F16 |
| R11 | VSS | F14 |
| R9 | VSS | F10 |
| R7 | VSS | F8 |
| R1 | VSS | F6 |
| P58 | VSS | F2 |
| P52 | VSS | E59 |
| P46 | VSS | E53 |
| P44 | VSS | E41 |
| P42 | VSS | E19 |
| P40 | VSS | E15 |
| P29 | VSS | E11 |
| P23 | VSS | E7 |
| P21 | VSS | E1 |
| P19 | VSS | D56 |
| P17 | VSS | D54 |
| P15 | VSS | D50 |
| P12 | VSS | D46 |
| P8 | VSS | D42 |
| P6 | VSS | D38 |
| N53 | VSS | D34 |
| N49 | VSS | D28 |
| N7 | VSS | C39 |
| N3 | VSS | C41 |
| M58 | VSS | C25 |
| M56 | VSS | C1 |
| M52 | VSS | B58 |
| M42 | VSS | B52 |
| M38 | VSS | B48 |
| M36 | VSS | B44 |
| M32 | VSS | B32 |
| M22 | VSS | B8 |
| M20 | VSS | B4 |
| M18 | VSS | B2 |
| M16 | VSS | A57 |
| M14 | VSS | A55 |
| M12 | VSS | A53 |
| L45 | VSS | A51 |
| L41 | VSS | A49 |
| L39 | VSS | A47 |
| K2 | VSS | A45 |
| L35 | VSS | A39 |
| L30 | VSS | A27 |
| L27 | VSS | A13 |
| L19 | VSS | A7 |
| L17 | VSS | A5 |
| L15 | VSS | A3 |
| L13 | VSS | |

CHERRY-TRAIL-GP-U



| CPU1H | SOC_CHV | 8 OF 11 |
|-------|---------|---------|
| BA37 | VSS | AD23 |
| BA35 | VSS | AK14 |
| BA28 | VSS | AK11 |
| K58 | VSS | AK7 |
| BA14 | VSS | AH58 |
| BA11 | VSS | AH48 |
| BA7 | VSS | AH54 |
| AY56 | VSS | AH52 |
| AY10 | VSS | AA40 |
| AY6 | VSS | AH44 |
| AW49 | VSS | AH42 |
| AW46 | VSS | AW7 |
| AW44 | VSS | AH29 |
| BB19 | VSS | AH17 |
| AW15 | VSS | AH15 |
| H36 | VSS | AH12 |
| AW9 | VSS | AH8 |
| AW7 | VSS | AH6 |
| AW5 | VSS | BV20 |
| AD46 | VSS | AG59 |
| AV58 | VSS | AG53 |
| AV8 | VSS | AG51 |
| D22 | VSS | AG49 |
| AU53 | VSS | AG11 |
| AU51 | VSS | AG7 |
| AU49 | VSS | AG5 |
| AU45 | VSS | AF58 |
| AU43 | VSS | AF54 |
| AU20 | VSS | AF43 |
| AU16 | VSS | AF31 |
| AU7 | VSS | AF16 |
| F40 | VSS | AF12 |
| AT54 | VSS | AF6 |
| AT52 | VSS | AF2 |
| F16 | VSS | AE7 |
| AT44 | VSS | AD56 |
| AT36 | VSS | AD54 |
| F8 | VSS | AD52 |
| AT34 | VSS | AD17 |
| AT27 | VSS | AD15 |
| AT25 | VSS | AD8 |
| AT17 | VSS | AD6 |
| AT15 | VSS | AC53 |
| AT12 | VSS | AC31 |
| AT6 | VSS | AC21 |
| E15 | VSS | AC19 |
| AR7 | VSS | AC15 |
| AR5 | VSS | AC43 |
| AP58 | VSS | AC39 |
| AP54 | VSS | AC37 |
| AP41 | VSS | AC35 |
| AP18 | VSS | AC22 |
| AP16 | VSS | AC16 |
| AP14 | VSS | AC14 |
| AP12 | VSS | AC11 |
| AP8 | VSS | AC9 |
| AP2 | VSS | AC7 |
| AN59 | VSS | AC1 |
| AN53 | VSS | AB58 |
| AN51 | VSS | AB6 |
| AN49 | VSS | AA49 |
| AN3 | VSS | AA46 |
| AM58 | VSS | AA44 |
| AM56 | VSS | AA32 |
| AM54 | VSS | AA38 |
| AM52 | VSS | AA17 |
| AM44 | VSS | AA15 |
| AM42 | VSS | AA11 |
| AM32 | VSS | AA3 |
| AM29 | VSS | Y56 |
| AM23 | VSS | Y12 |
| AM17 | VSS | Y10 |
| AM15 | VSS | Y8 |
| AM12 | VSS | Y2 |
| AM6 | VSS | W53 |
| AK59 | VSS | W45 |
| AK57 | VSS | W43 |
| AK55 | VSS | W41 |
| AK53 | VSS | W40 |
| AK45 | VSS | W16 |
| AK43 | VSS | W14 |
| AK26 | VSS | W7 |
| | VSS | G35 |

CHERRY-TRAIL-GP-U



| CPU1I | SOC_CHV | 9 OF 11 |
|-------|---------|---------|
| B88 | VSSA | BL13 |
| BK24 | VSS | BL7 |
| BW57 | VSS | BL5 |
| BW55 | VSS | BK58 |
| BW53 | VSS | BK54 |
| BW51 | VSS | BK50 |
| BW49 | VSS | BK48 |
| BW47 | VSS | BK6 |
| BW45 | VSS | BK2 |
| BW39 | VSS | BJ45 |
| BW30 | VSS | BJ41 |
| BW19 | VSS | BJ39 |
| BW7 | VSS | BJ35 |
| BW5 | VSS | BJ27 |
| BW3 | VSS | BJ23 |
| BV58 | VSS | BJ17 |
| BV52 | VSS | BJ13 |
| BV48 | VSS | BJ11 |
| BV44 | VSS | BH58 |
| BV20 | VSS | BH56 |
| BV16 | VSS | BH52 |
| BV12 | VSS | BH42 |
| BV8 | VSS | BH38 |
| BV6 | VSS | BH20 |
| BV2 | VSS | BH12 |
| BV59 | VSS | BH8 |
| BU11 | VSS | BH2 |
| BU3 | VSS | BG53 |
| BU1 | VSS | BG49 |
| BT56 | VSS | BG7 |
| BT54 | VSS | BG5 |
| BT50 | VSS | BF58 |
| BT46 | VSS | BF52 |
| BT42 | VSS | BF46 |
| BT38 | VSS | BF44 |
| BT34 | VSS | BF42 |
| BT28 | VSS | BF40 |
| BT24 | VSS | BF34 |
| BT20 | VSS | BF36 |
| BT16 | VSS | BF32 |
| BT12 | VSS | BF27 |
| BT8 | VSS | BD16 |
| BR59 | VSS | BA1 |
| BR53 | VSS | BF21 |
| BR41 | VSS | BF19 |
| BR6 | VSS | BF17 |
| BR1 | VSS | BF15 |
| BP58 | VSS | BF12 |
| BP48 | VSS | BF6 |
| BP40 | VSS | BE59 |
| BP32 | VSS | BE57 |
| BP26 | VSS | BE11 |
| BP18 | VSS | BE7 |
| BP10 | VSS | BE1 |
| BP6 | VSS | BD56 |
| BN53 | VSS | BD45 |
| BN45 | VSS | BD43 |
| BN41 | VSS | BD41 |
| BN39 | VSS | BD18 |
| BN35 | VSS | BD12 |
| BN30 | VSS | BD6 |
| BN27 | VSS | BC59 |
| BN23 | VSS | BC53 |
| BN21 | VSS | BC51 |
| BN17 | VSS | BC49 |
| BN13 | VSS | BC11 |
| BN7 | VSS | BC7 |
| BM56 | VSS | BC5 |
| BM46 | VSS | BB58 |
| BM44 | VSS | BB54 |
| BM40 | VSS | BB52 |
| BM36 | VSS | BB46 |
| BM34 | VSS | BB44 |
| BM28 | VSS | BB42 |
| BM26 | VSS | BB10 |
| BM22 | VSS | BB6 |
| BM18 | VSS | BA53 |
| BM16 | VSS | BA45 |
| BM10 | VSS | BA43 |
| BL41 | VSS | BA41 |
| BL30 | VSS | D20 |
| BL23 | VSS | L33 |
| M34 | VSS | |

CHERRY-TRAIL-GP-U



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Blackwell T4

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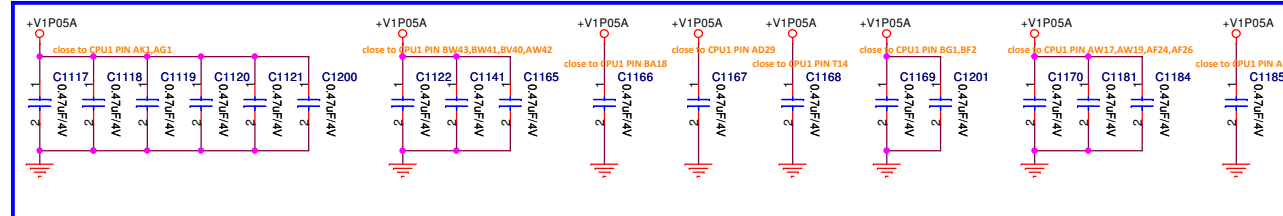
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Title
10_SOC (VSS)

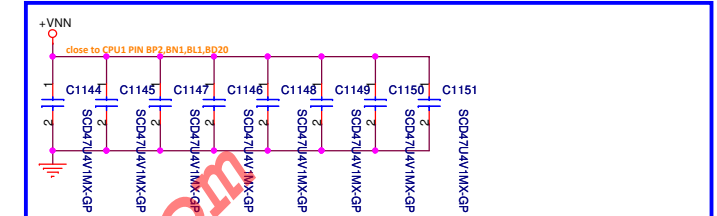
| | | |
|------|---------------------------------|-----------|
| Size | Document Number Blackwell T4 | Rev -1 |
|------|---------------------------------|-----------|

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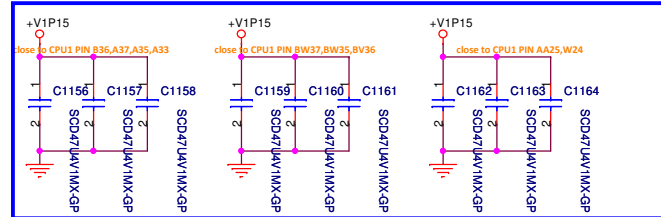
+V1P05A



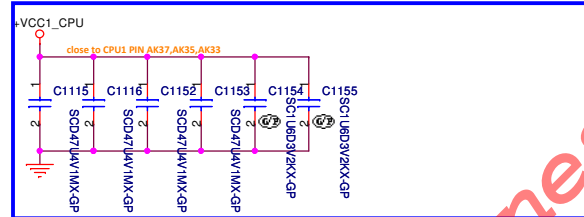
+VNN



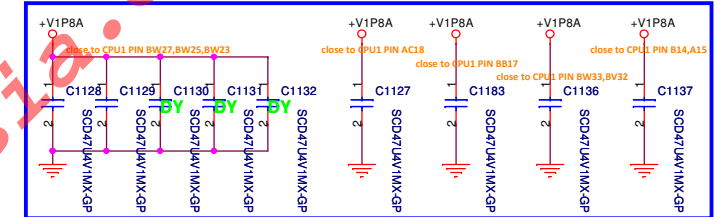
+V1P15



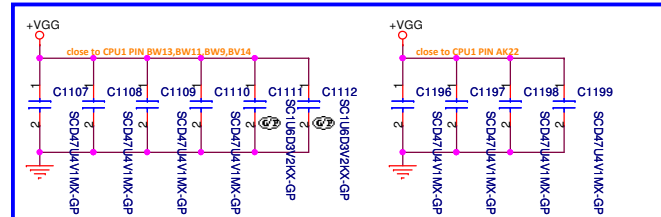
+VCC1_CPU



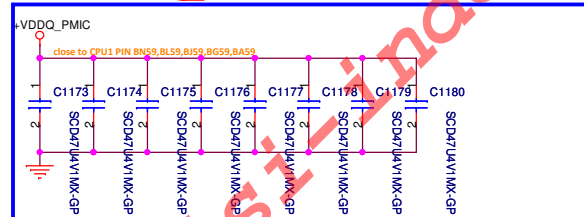
+V1P8A



+VGG



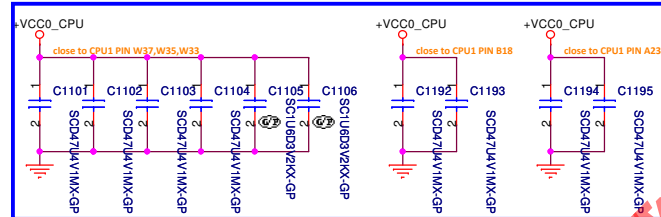
+VDDQ_PMIC



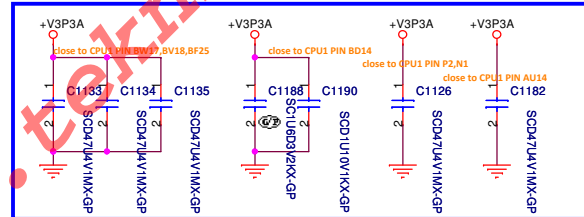
+V1P2A



+VCC0_CPU



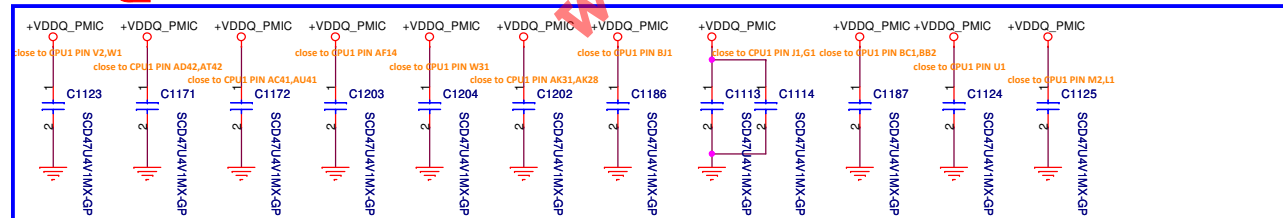
+V3P3A



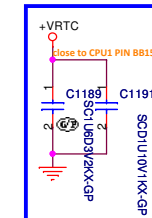
+VSDIO



+VDDQ_PMIC



+VRTC



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Title 11_CPU (VLV2 Decoupling)

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Date: Thursday, October 01, 2015

Sheet 11 of 73

Rev

-1

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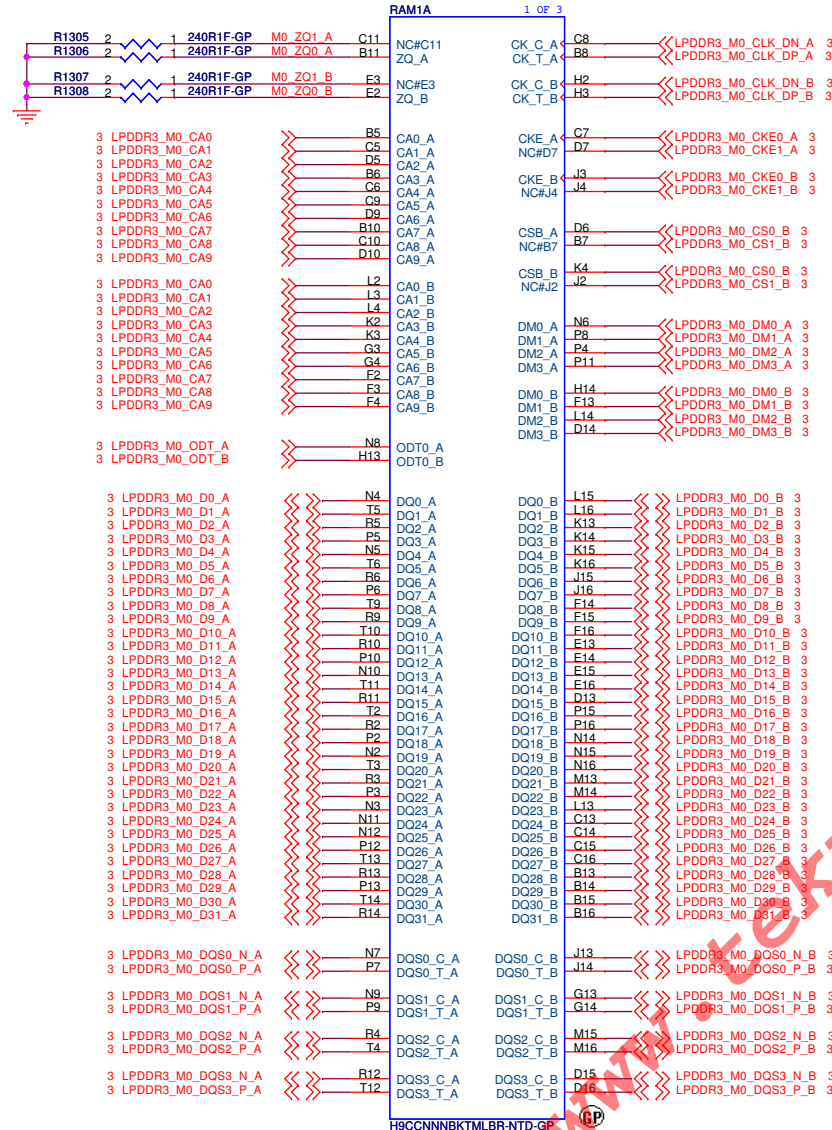
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| Title 12_LPDDR3 (Reserved) | | | |
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| | Blackwell T4 | | -1 |
| Date: Thursday, October 01, 2015 | | Sheet 12 | of 73 |

LPDDR3 MEMORY CHANNEL A

SSID=MEMORY

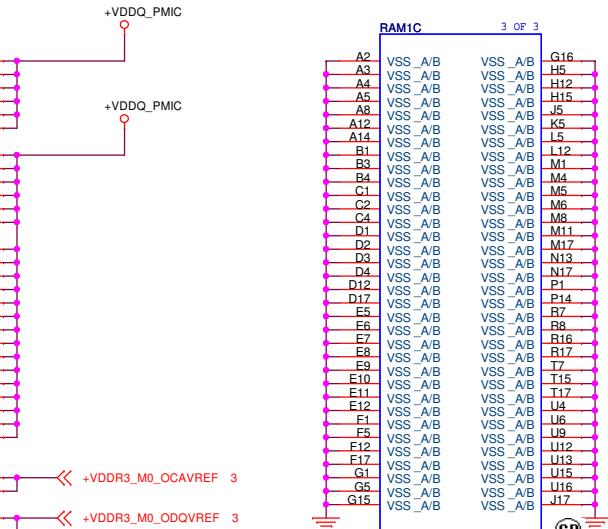
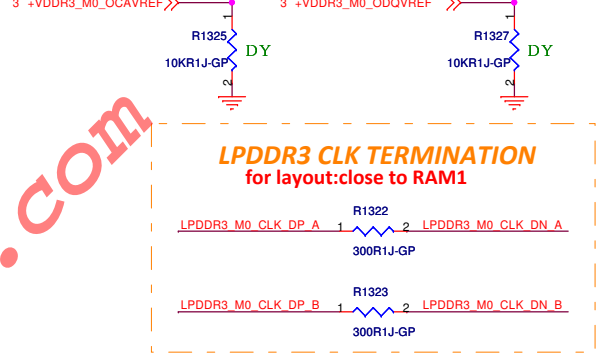
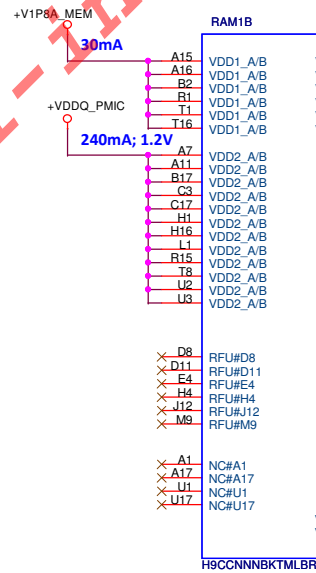
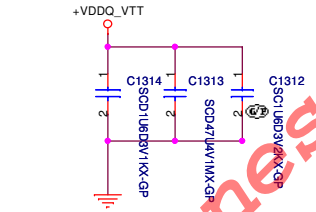
H9CCNNN8KTMBR-NTM-GP



for layout:
colsed to RAM1



LPDDR3 CA TERMINATION



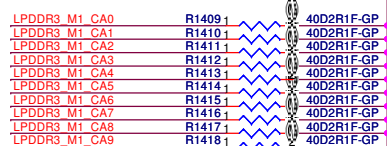
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LPDDR3 MEMORY CHANNEL B

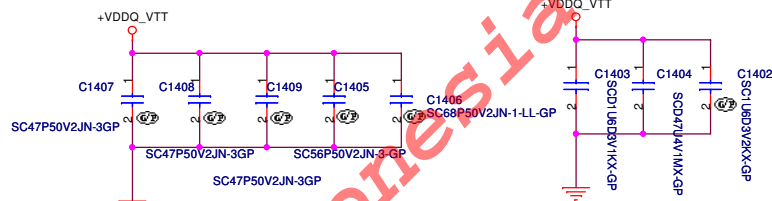
SSID=MEMORY

H9CCNNN8KTMBR-NTM-GP

for layout:
close to RAM2

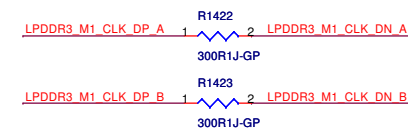


LPDDR3 CA TERMINATION



LPDDR3 CLK TERMINATION

for layout: close to RAM2



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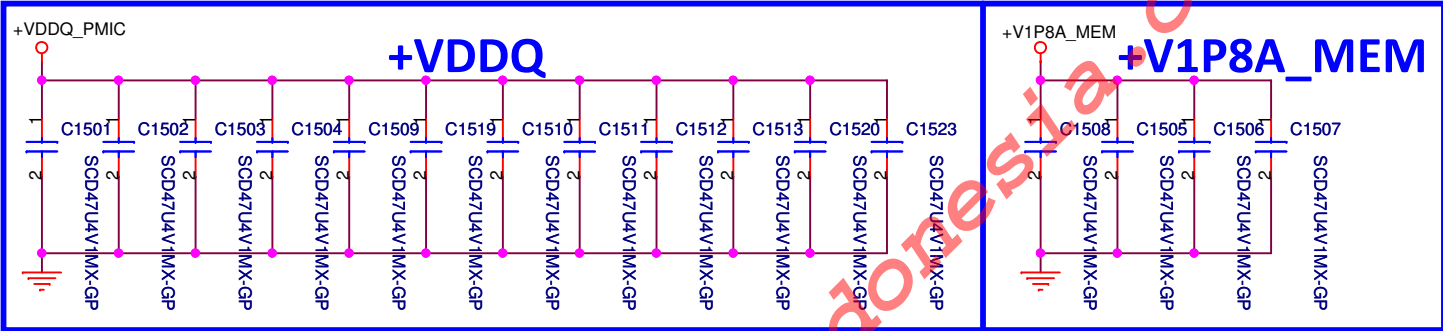
14 LPDDR3_RAM2(H9CCNNN8KTMLBR)

Size Document Number Rev
Blackwell T4 -1
Date: Thursday, October 01, 2015 Sheet 14 of 73

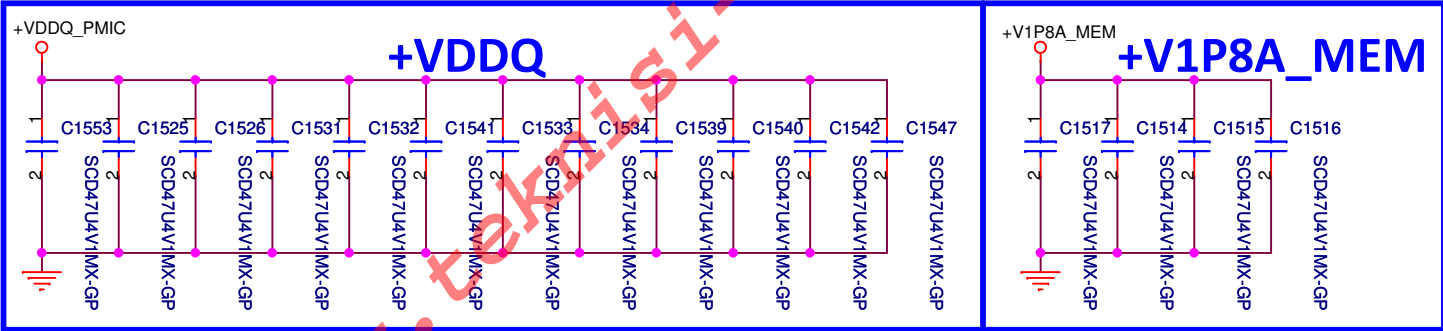
LPDDR3 DECOUPLING CAPACITORS

SSID=MEMORY

LPDDR3 MEMORY CHANNEL A



LPDDR3 MEMORY CHANNEL B



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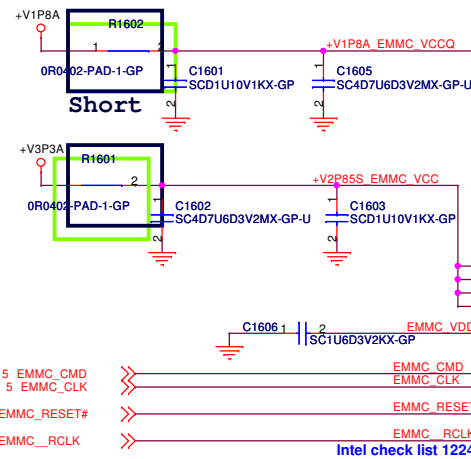
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| Title 15_LPDDR3_TERMINATIONS | | | |
| Size | Document Number | Rev | |
| | Blackwell T4 | -1 | |
| Date: Thursday, October 01, 2015 | | Sheet | 15 of 73 |

eMMC SSID=EMMC

Samsung - 16GB - KLMAG2GEAC-B031
 PN : 072.KMAG2.0B0U
 Samsung - 32GB - KLMBG4GEAC-B031
 PN : 072.KMBG4.000U



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64GB
 072.KMCG8.0B0U

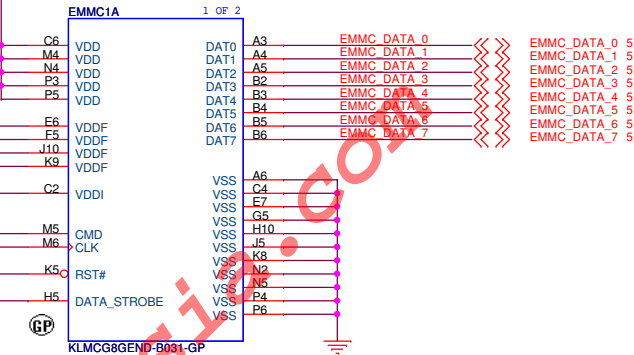
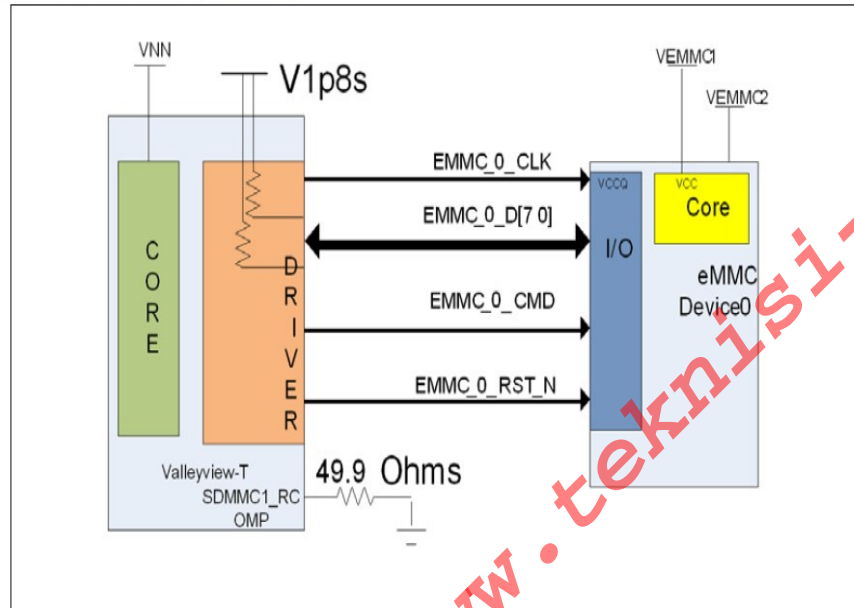


Figure 3-44.eMMC Interface Topology

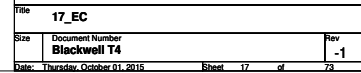


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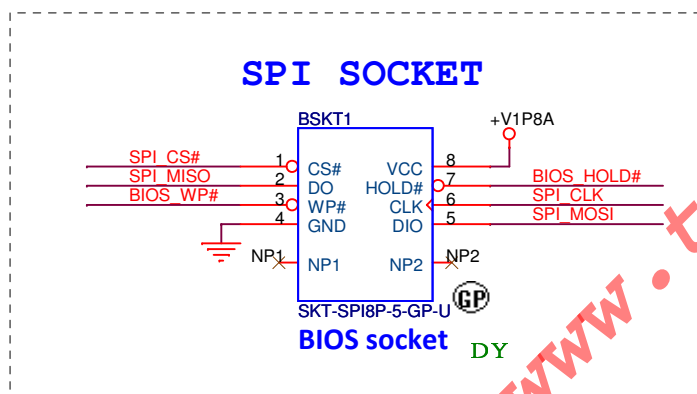
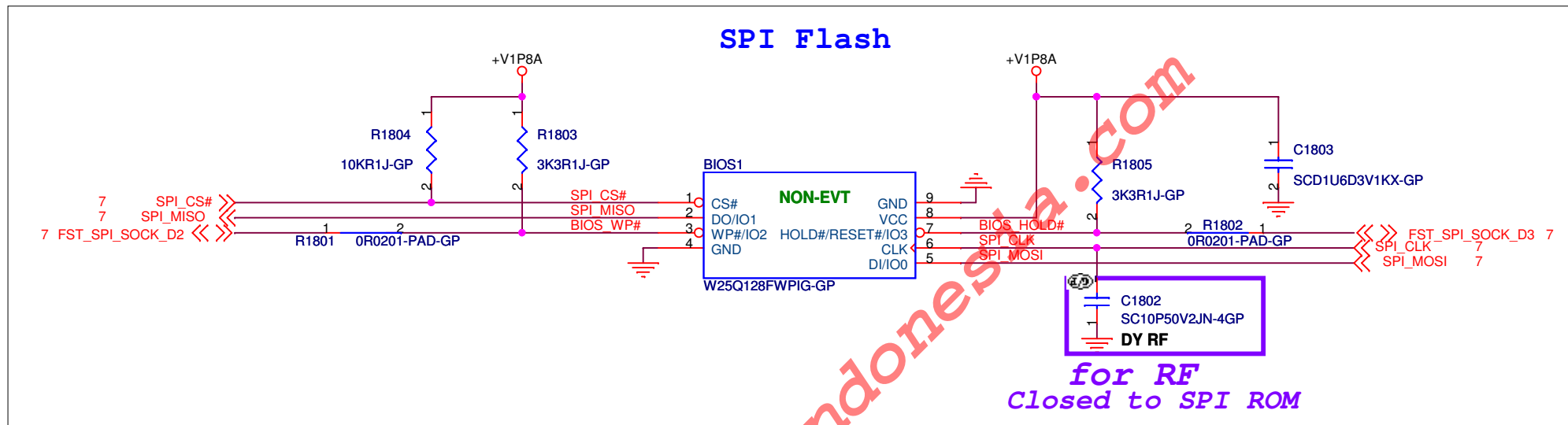
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| Title 16_eMMC | | |
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SPI ROM SSID=Flash.ROM

Need to made FPC for new debug port.



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Title

18_ SPI NOR

Size

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Sheet 18 of 73

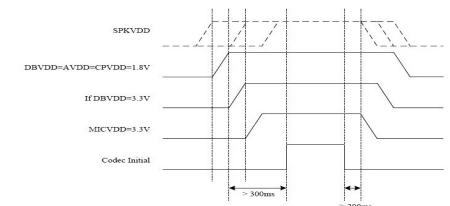
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| Title 19_Thermal Protect(Reserved) | | | |
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SSID=AUDIO



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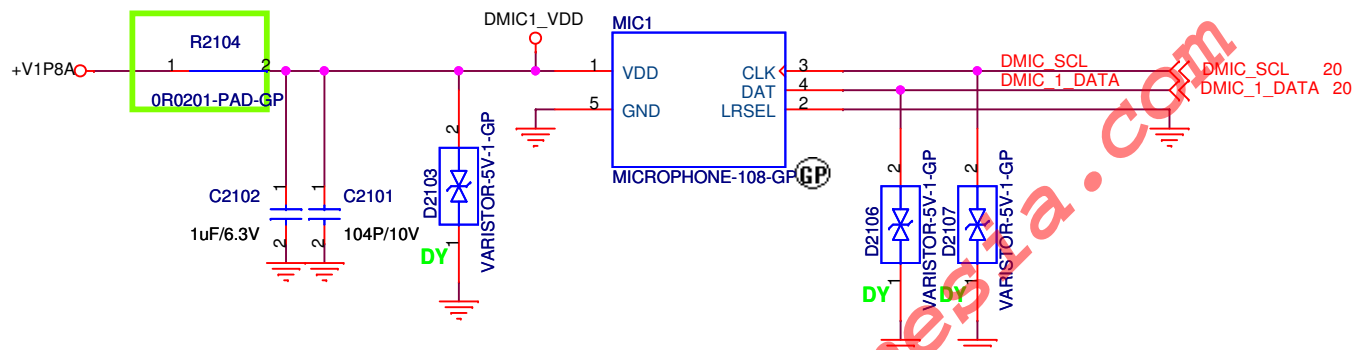
Sheet 20 of 73

-1

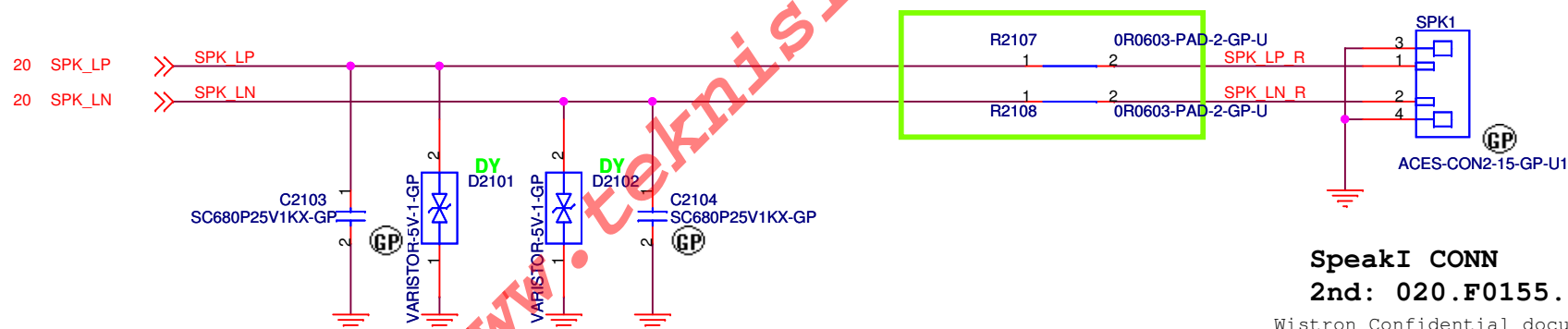
DMIC

SSID=AUDIO

need to check DMIC position and SEL pin define



SPEAKER



SpeakI CONN

2nd: 020.F0155.0004

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<Core Design>

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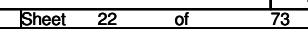
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Taipei Hsien 221, Taiwan, R.O.C.Title
21_AUDIO AMP/DMIC/SPKSize
Document Number
Blackwell T4Rev
-1

Date: Thursday, October 01, 2015

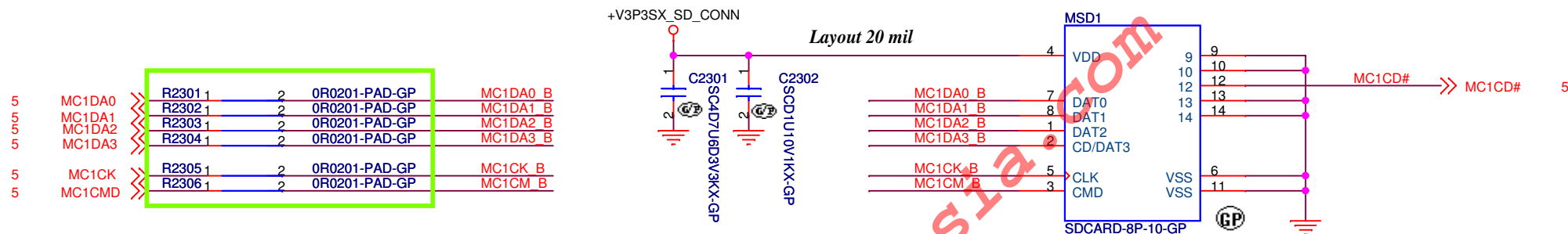
Sheet 21 of 73

SSID=AUDIO

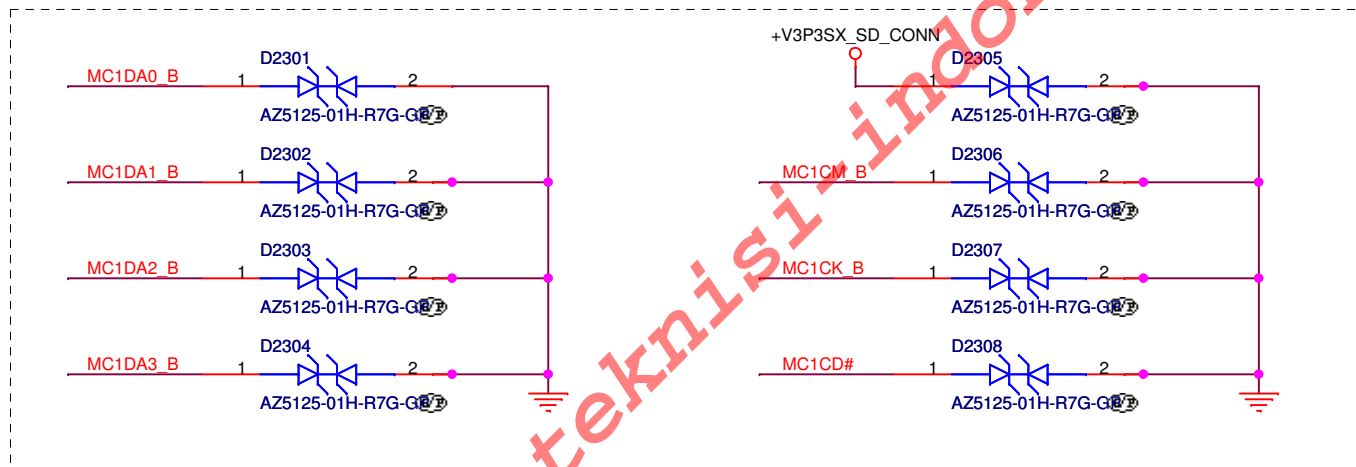


SD CARD

SSID=SDIO



for ESD/RF Closed to SDC1



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Title 23_uSD Card CONN

Size Document Number Blackwell T4

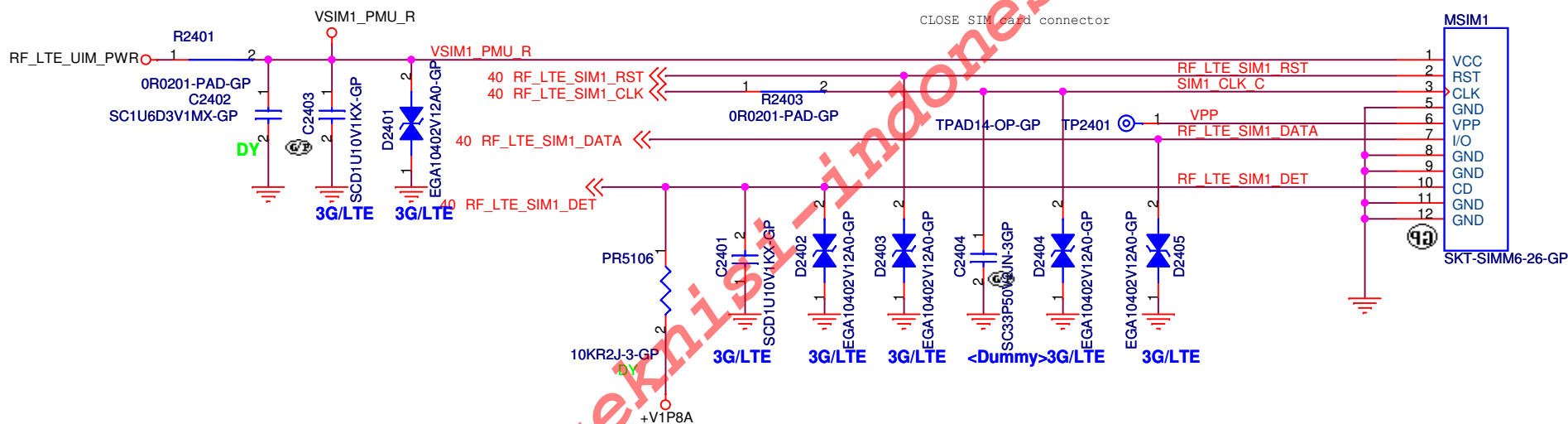
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Sheet 23 of 73

SIM CARD

SSID=Wireless



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Title
24_uSIM CONN

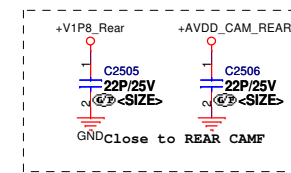
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Blackwell T4

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Date: Thursday, October 01, 2015

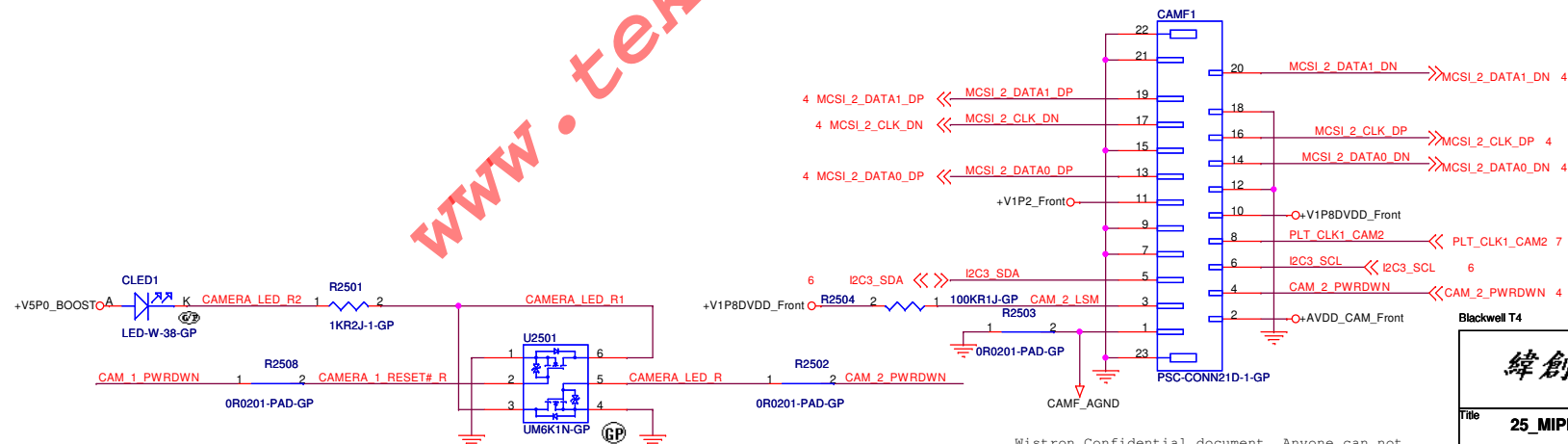
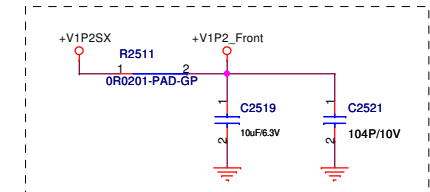
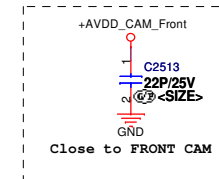
Sheet 24 of 73

SSID=CAMERA



The schematic diagram illustrates the electrical connections for the CAM1 module to the HRS-CONN30E-2-GP connector. Key connections include:

- Power Supply:**
 - $+V2P8_CAM_VCMO$ connected to pin 30.
 - $+V1P2_Rear$ connected to pin 16 via resistor $R2517$ and a green triangle symbol.
 - $+AVDD_CAM_REAR$ connected to pin 19.
 - $+V1P8_Rear$ connected to pin 18.
 - DV (diode) connected to pin 2.
 - $FSIN_REAR$ connected to pin 21.
 - $DVDD_REAR$ connected to pin 17.
- Signal Lines:**
 - $I2C3_SCL$ and $I2C3_SDA$ connected to pins 2 and 1 via resistors $R2506$ and $R2505$, and the $0R2021-PAD-GP$ component.
 - PLT_CLK1_CAM1 connected to pin 25.
 - $CAM1_PWRDWN$ connected to pin 23.
 - $MCSI_1_DATA1_DN$ and $MCSI_1_DATA1_DP$ connected to pins 2 and 3.
 - $MCSI_1_DATA0_DN$ and $MCSI_1_DATA0_DP$ connected to pins 5 and 6.
 - $MCSI_1_CLK_DN$ and $MCSI_1_CLK_DP$ connected to pins 7 and 8.
- Grounding:**
 - Pin 15 is connected to ground.
 - Pin 16 is connected to ground via resistor $R2517$ and a green triangle symbol.
 - Pin 22 is connected to ground.



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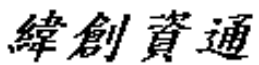
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| Title <div>26_Camera_3D</div> | | |
| Size | Document Number <div>Blackwell T4</div> | Rev <div>-1</div> |
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Title

28_Full/MICRO USB CONN(Reserved)

Size

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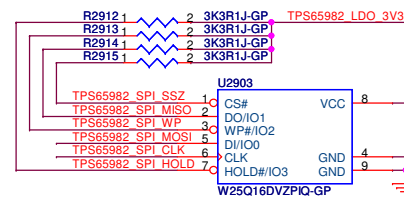
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SSID=USB

LEVEL SHIFT

6 CPU_USB_OC# << CPU_USB_OC# D2901 A >> K DB2U31600L-GP TPS65982 GPIO8

FLASH



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| Title | 29 USB TYPE C 1 |
|-------|------------------------|

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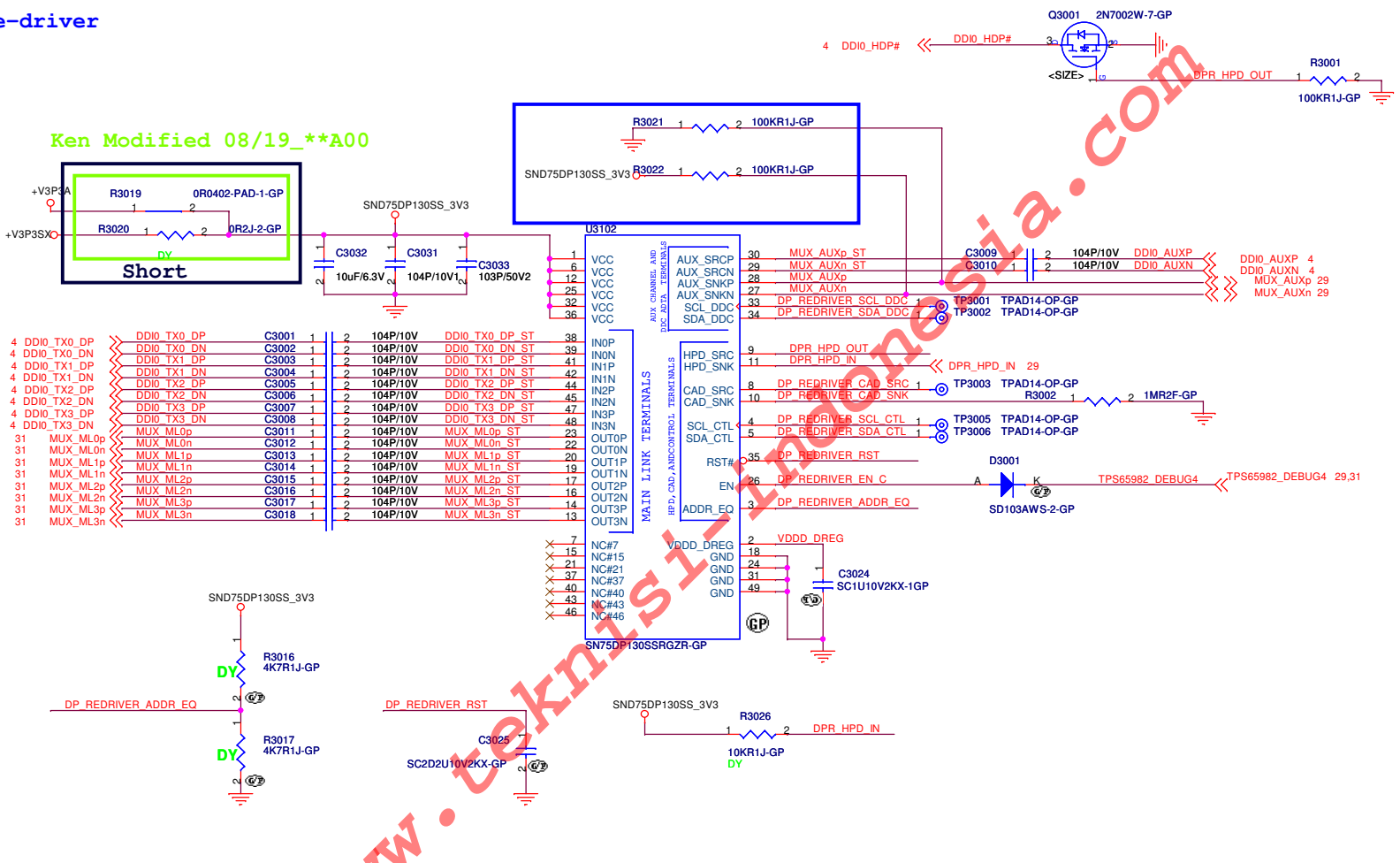
Sheet 29 of 73

-1

SSID=VIDEO

Re-driver

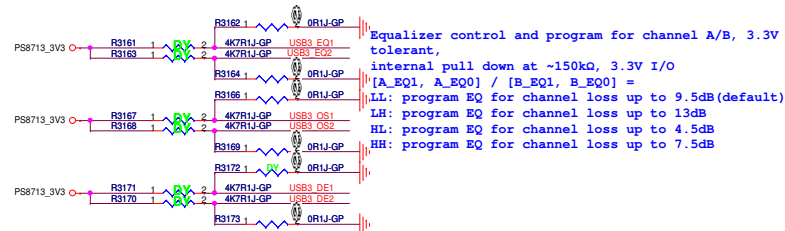
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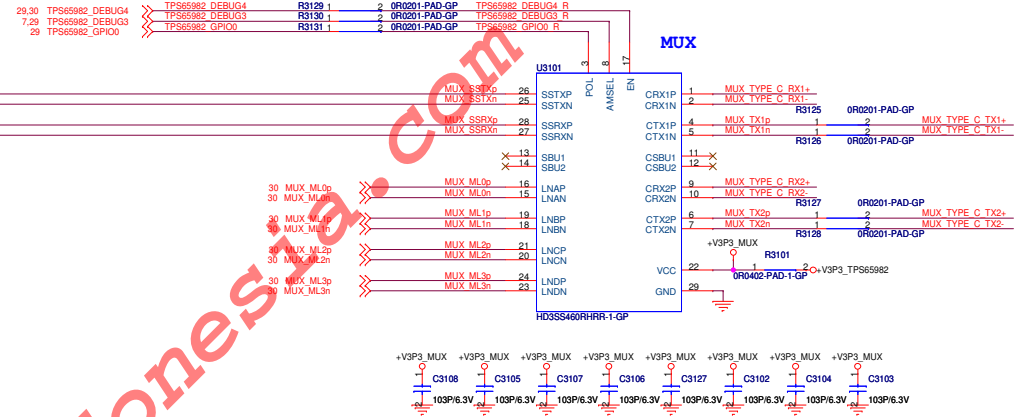
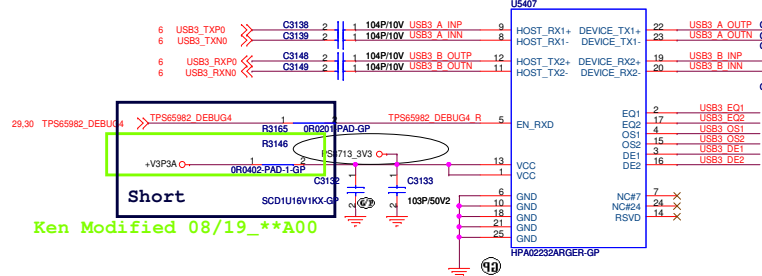
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|-------|----------------------------|-----------------|
| Title | | 30_USB_TYPE_C_2 |
| Size | Document Number | Blackwell T4 |
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| Rev | | -1 |



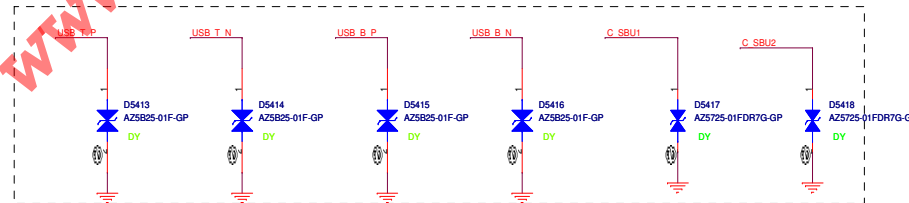
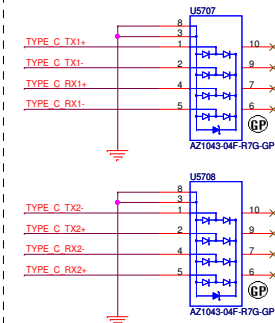
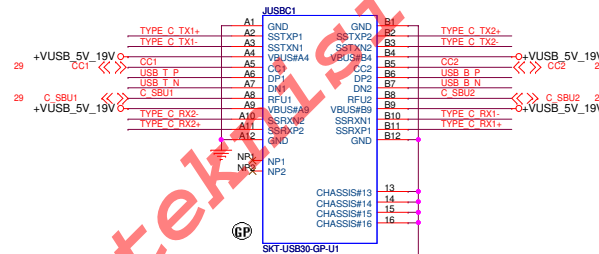
Programmable output pre-emphasis level setting for channel A/B, 3.3V tolerant, internal pull down at ~150kΩ
 $[A_DE1, A_DE0] / [B_DE1, B_DE0] =$
 LL: 3.5dB de-emphasis (default)
 LH: No de-emphasis
 HL: 2.7dB de-emphasis
 HH: 5dB de-emphasis

LFPS swing adjust, 3.3V tolerant, internal pull down at ~150kΩ
 L: normal LFPS swing (default)
 H: tune down LFPS swing

USB3.0 re-Driver



TYPE-C Connector



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| Title 32_USB HUB(Reserved) | | | |
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Vibrator

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Title

33_Vibrator(Reserved)

Size

Document Number

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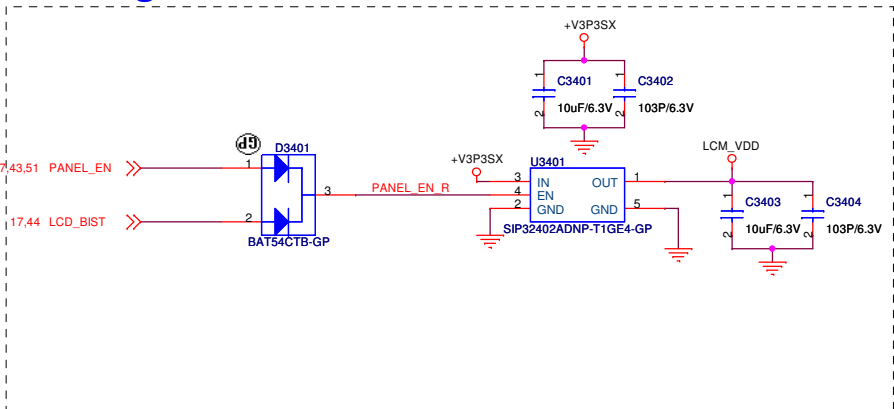
Rev

-1

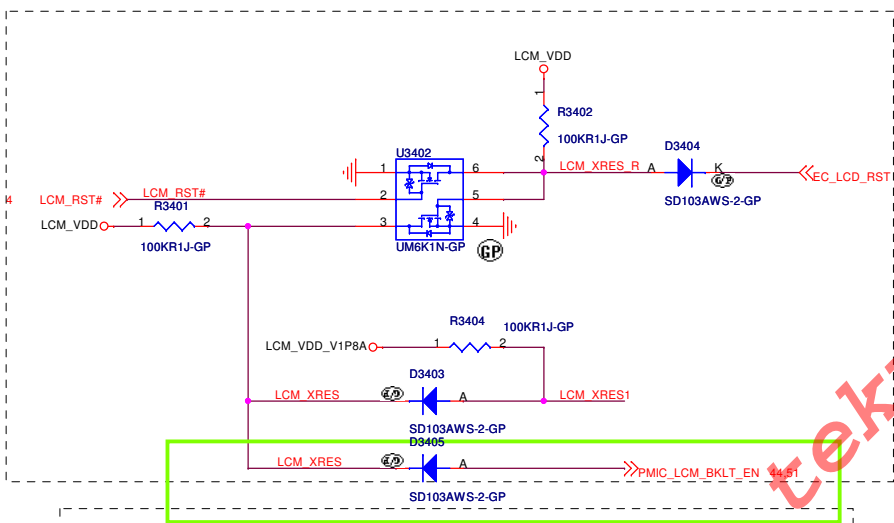
Date: Thursday, October 01, 2015

Sheet 33 of 73

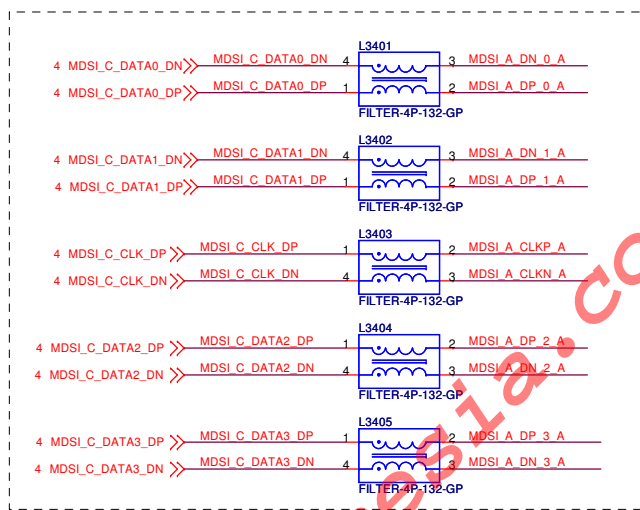
LCM Logic Power



Level Shift



For EMI

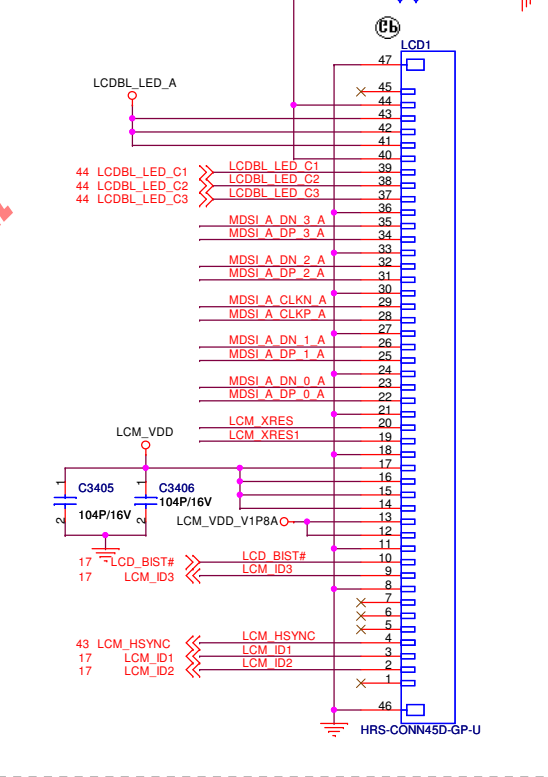


LCM ID 改的目的: 當EC 有電, 就可以偵測LCM是哪家

| LCM ID3 | LCM ID2 | LCM ID1 | Vendor |
|---------|---------|---------|-----------|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | AUO-WUXGA |
| 0 | 1 | 0 | BOE-WUXGA |
| 0 | 1 | 1 | AUO-WUXGA |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | BOE-WXGA |
| 1 | 1 | 1 | AUO-WXGA |

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LCM Conector



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Title 34_MIPI_LCM_CONN

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Sheet 34

of 73

Rev
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| Title 35_uHDMI CONN(Reserved) | | |
| Size | Document Number Blackwell T4 | Rev -1 |
| Date: Thursday, October 01, 2015 | | |
| Sheet 35 of 73 | | |

Blanking

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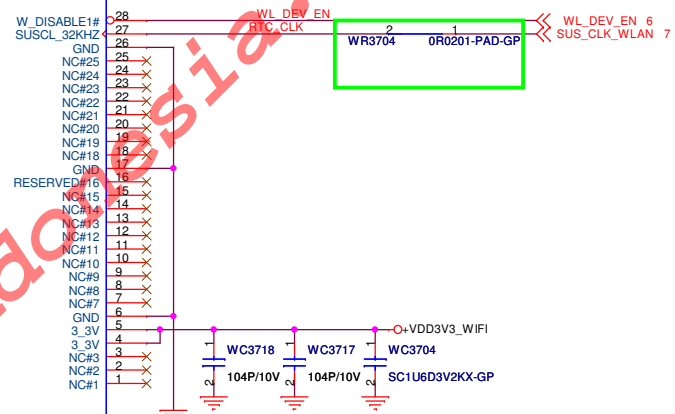
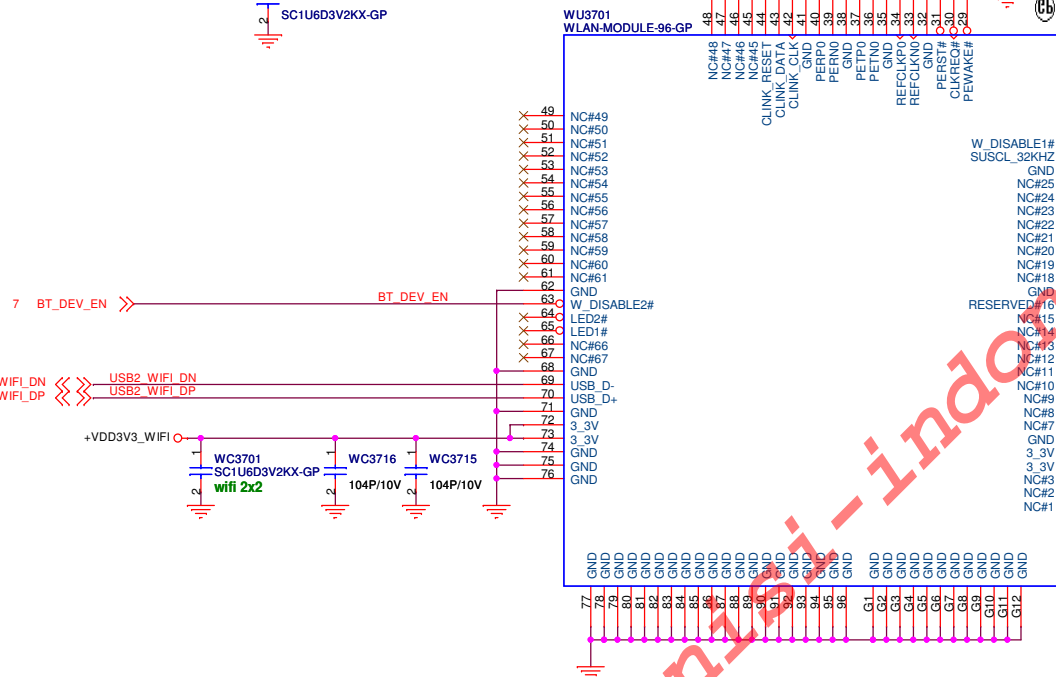
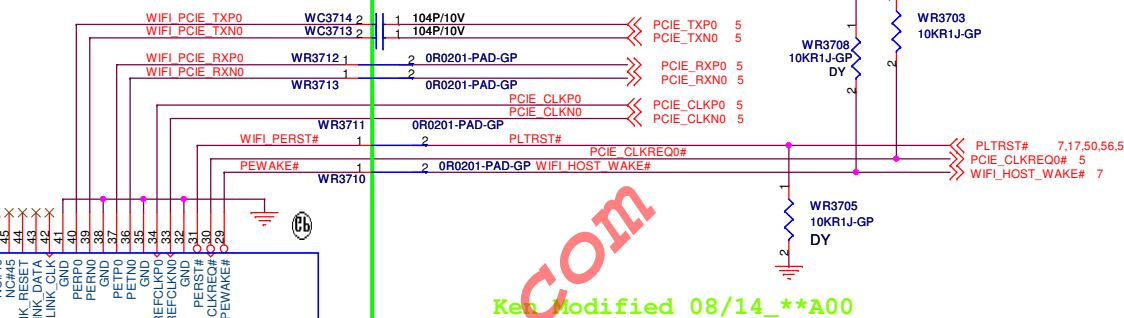
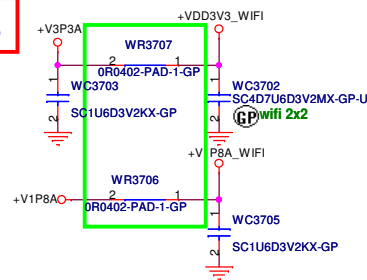
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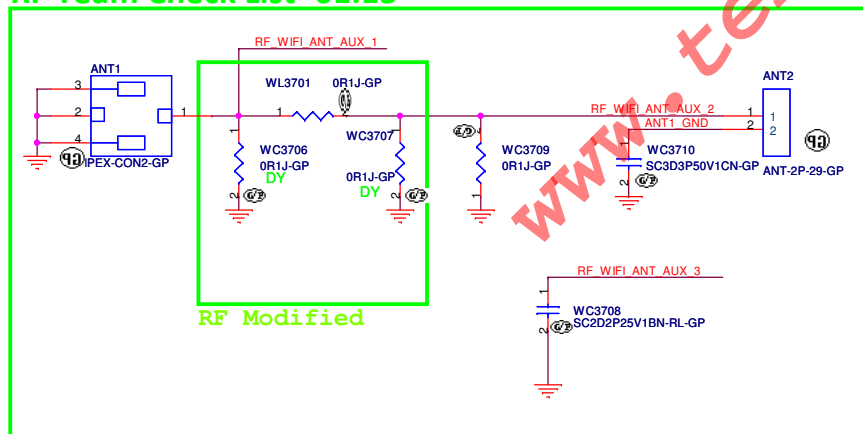
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|--|---------------------|-------------------------|
| <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> | | |
| Title 36_Display Port(Reserved) | | |
| Size | Document Number | Rev |
| | Blackwell T4 | -1 |
| Date: Thursday, October 01, 2015 | | Sheet 36 of 73 |

WIFI/BT 2X2 USI

SSID=Wireless



RF Team Check List -01.13



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| | | |
|-------|----------------------------|----------------|
| Title | | 37_WIFI/BT |
| Size | Document Number | Blackwell T4 |
| Date | Thursday, October 01, 2015 | Sheet 37 of 73 |

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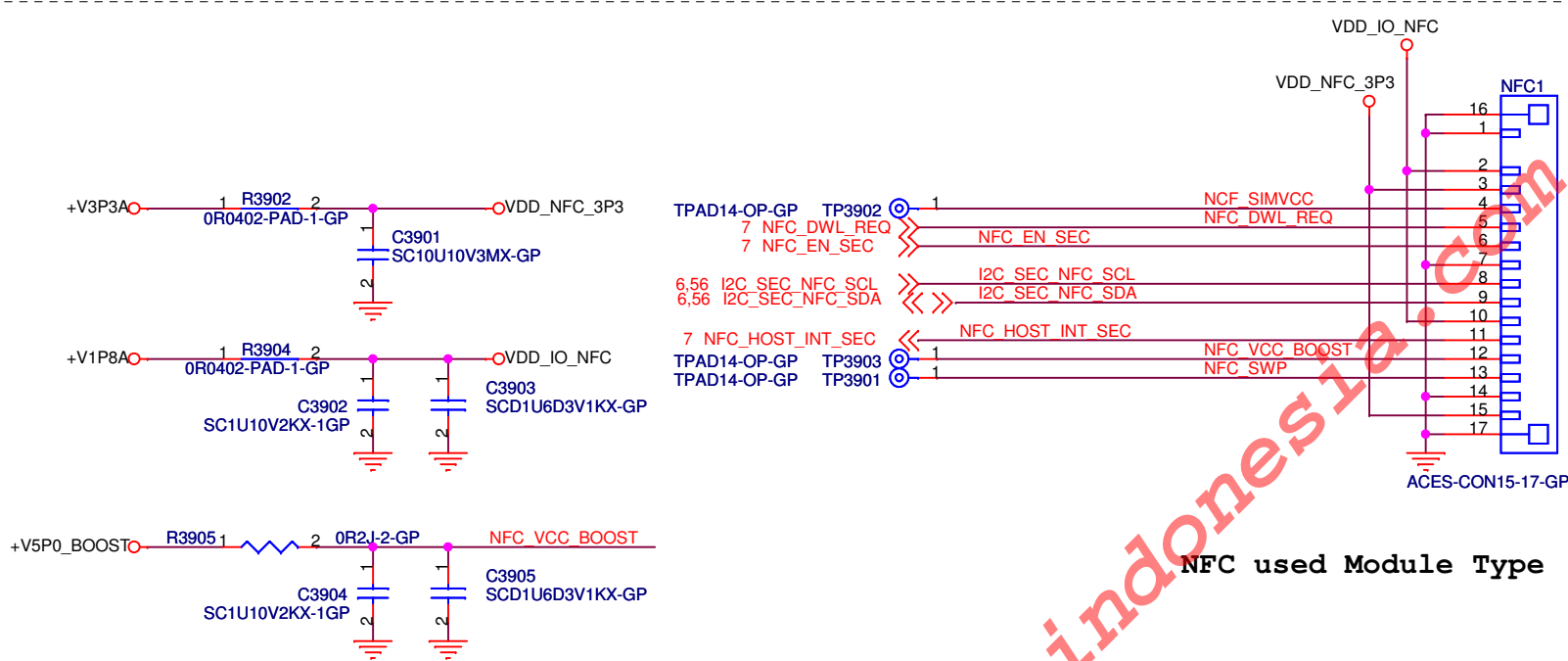
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| | | |
|--|--|-------------------------|
| <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> | | |
| Title 38_GPS(Reserved) | | |
| Size | Document Number Blackwell T4 | Rev -1 |
| Date: Thursday, October 01, 2015 | | Sheet 38 of 73 |

NFC

SSID=NFC



| Pin number | Name |
|------------|----------------------|
| 1 | MOD_VDD |
| 2 | MOD_GND |
| 3 | SWP |
| 4 | VCC_BOOST |
| 5 | IRQ |
| 6 | PMUVCC |
| 7 | I ² C_SDA |
| 8 | I ² C_SCL |
| 9 | MOD_GND |
| 10 | Reset/Wakeup |
| 11 | DWL_REQ |
| 12 | SIMVCC |
| 13 | MOD_VDD |
| 14 | VDD_IO |
| 15 | MOD_GND |

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Title
39_NFC

Size Document Number
Blackwell T4

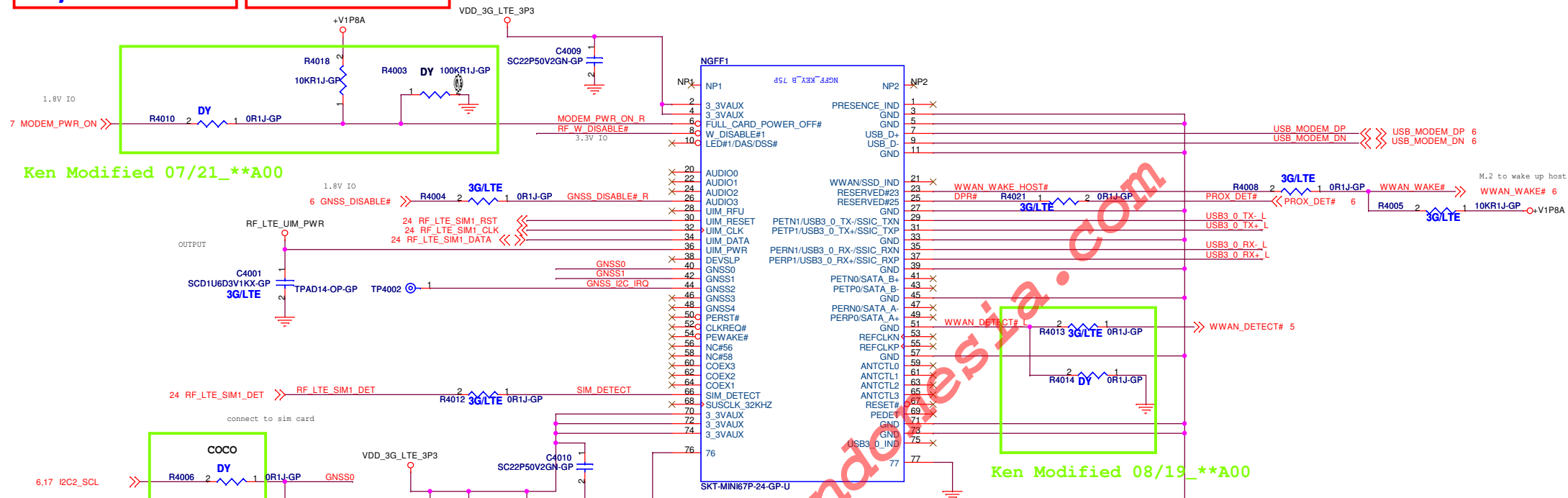
Rev
-1

Date: Thursday, October 01, 2015

Sheet 39 of 73

3G/LTE module

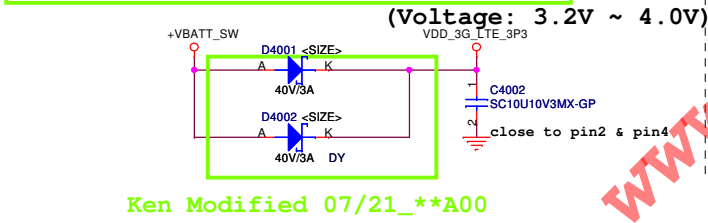
SSID=Wireless



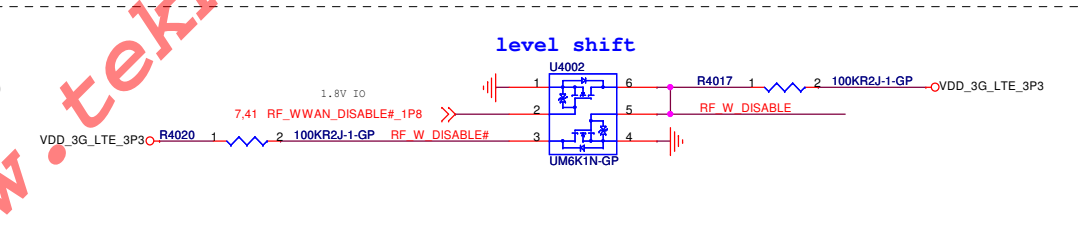
Ken Modified 07/21_**A00

Ken Modified 08/19_**A00

DW5811 EM7455 (Non COCO)
 DW5808 EM7355 (COCO)
 DW5809, DW5808: R4006, R4007, R4009: DY

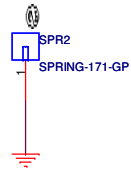


Ken Modified 07/21_**A00

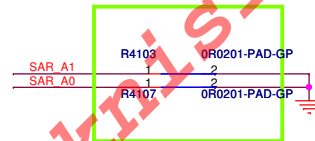
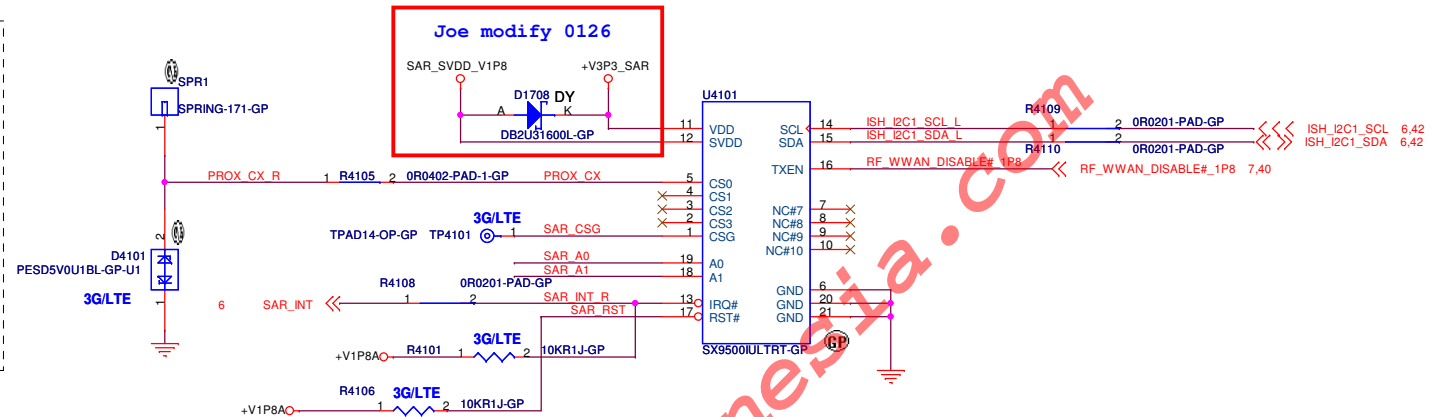


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SSID=User.Interface



| A1 | A0 | Address |
|----|----|---------|
| 0 | 0 | 0x28 |
| 0 | 1 | 0x29 |
| 1 | 0 | 0x2A |
| 1 | 1 | 0x2B |

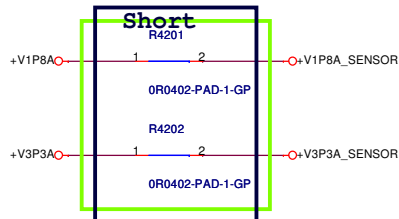


Sheet 41 of 73

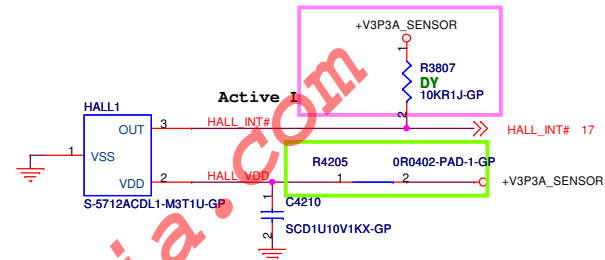
Sensor

SSID=User.Interface

Ken Modified 08/19_**A00

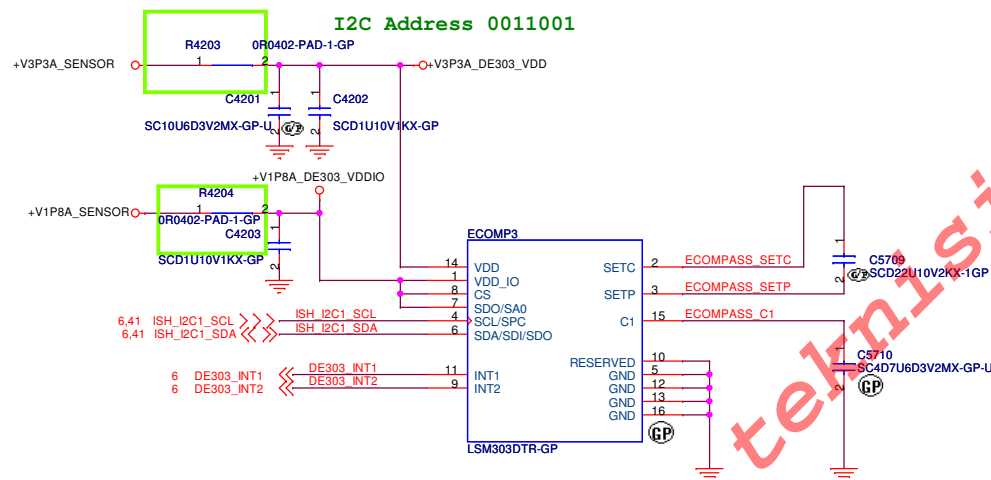


HALL Sensor

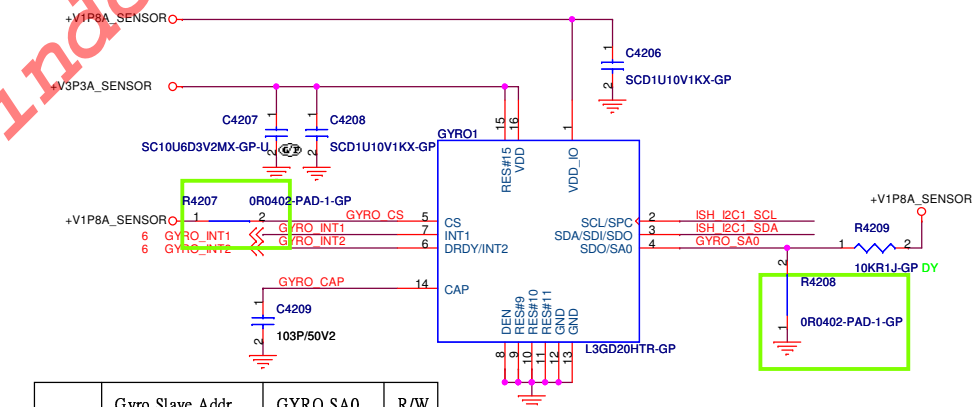


G Sensor + E-Compass

I2C Address 0011001



Gyro Sensor I2C Address 1101010



| | Gyro Slave Addr | GYRO SA0 | R/W |
|----|-----------------|----------|-----|
| D4 | Write | 110101 | 0 |
| D5 | Read | 110101 | 0 |
| | | | 1 |

| | G-Sensor Slave Addr | R/W |
|----|---------------------|----------|
| 3A | Write | 0011,101 |
| 3B | Read | 0011,101 |

| | c-Compass Slave Addr | R/W |
|----|----------------------|----------|
| 3C | Write | 0011,110 |
| 3D | Read | 0011,110 |

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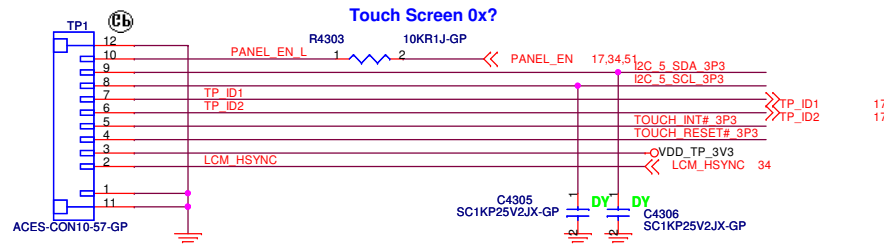
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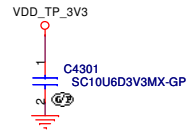
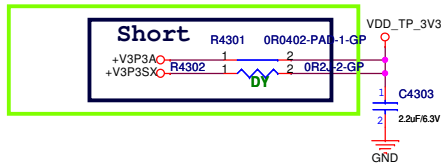
| | |
|-------|----------------------------|
| Title | 42_Sensor |
| Size | Document Number |
| | Blackwell T4 |
| Date | Thursday, October 01, 2015 |
| Sheet | 42 of 73 |
| Rev | -1 |

Touch Panel

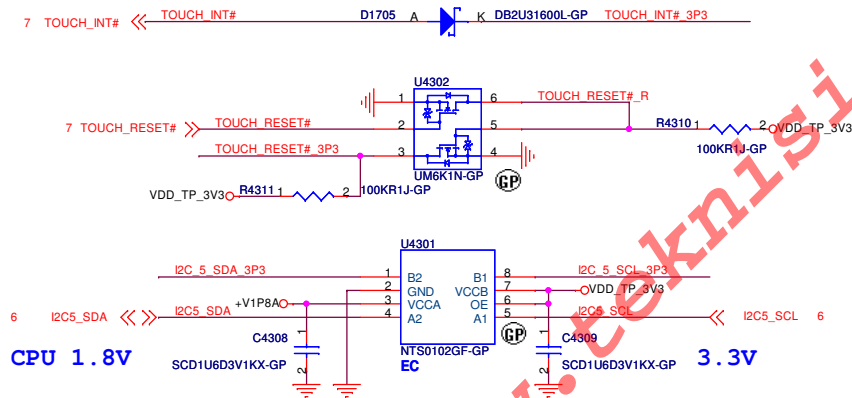
SSID=Touch.Panel



Ken Modified 08/19_**A00



Level shift



| CN1 PIN # | Host 接續時 | Description |
|-----------|-----------|--|
| 1 | NC | Keep Open |
| 2 | SDA | IIC Data Open drain; pull-up resistor at Host is needed |
| 3 | SCL | IIC Clock Open drain; pull-up resistor at Host is needed |
| 4 | ID01 | Touch Sensor Identification Pin 01 |
| 5 | ID02 | Touch Sensor Identification Pin 02 |
| 6 | IRQ | IIC Data Ready Output "LOW" when data ready to send Open drain; pull-up resistor at Host is needed |
| 7 | RESET | RESET Stop operation when pull "LOW" Build-in pull-up resistor 100kohm |
| 8 | VDD +3.3V | 3.3volt power input |
| 9 | HSYNC | LCD Hsync input |
| 10 | GND | Ground |

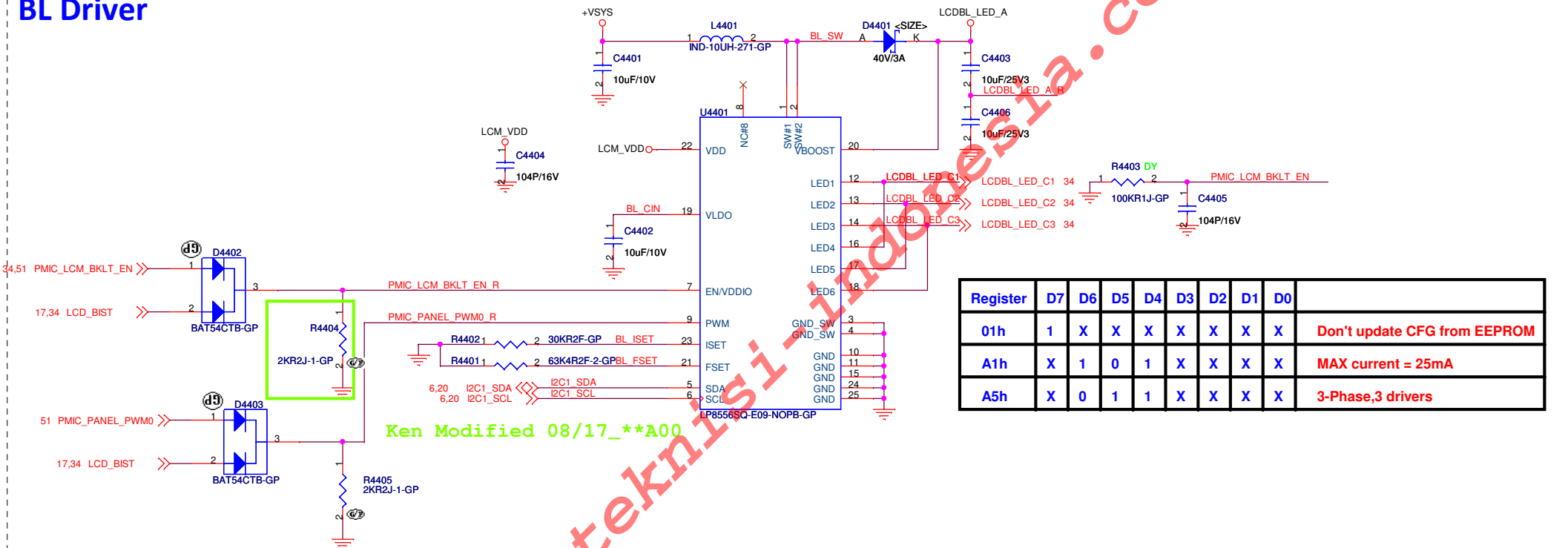
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| | | | |
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| Title 43_Touch Panel | | | |
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SSID=VIDEO

BL Driver



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Title 44_LED BOOST

Size B Document Number Blackwell T4

Rev -1

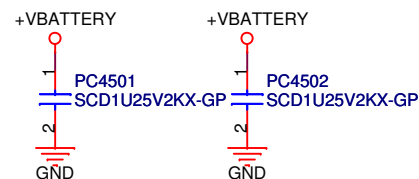
Date: Thursday, October 01, 2015

Sheet 44 of 73

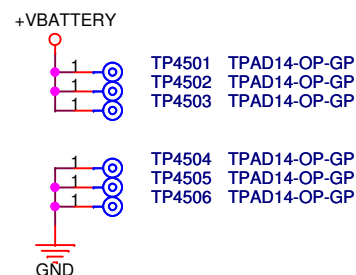
BATTERY CONN

SSID=PWR.Support

For EMI



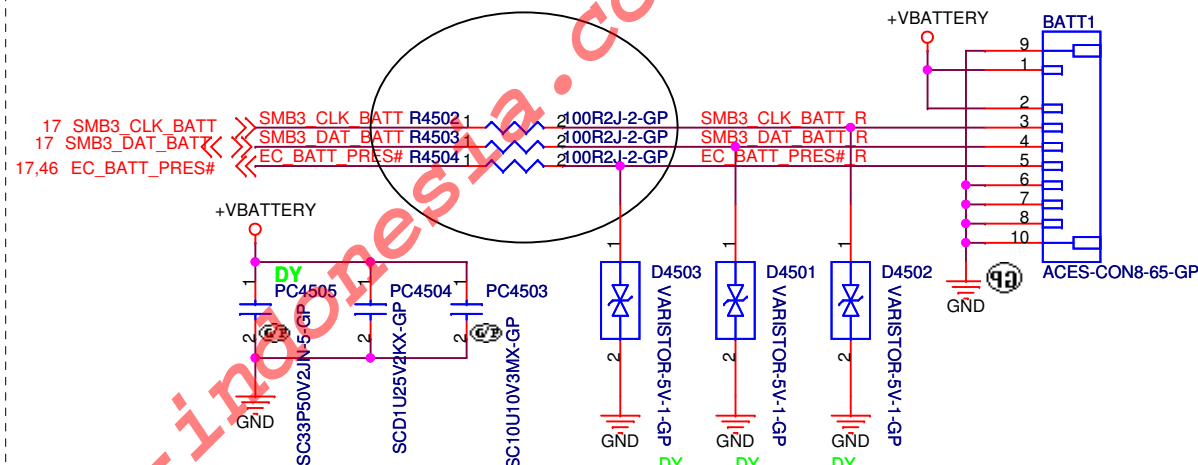
For Test



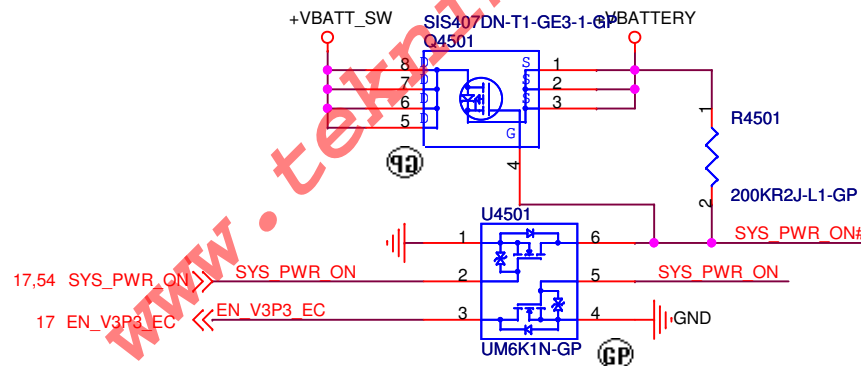
Battery Connector

12.28 Ken Modified

Battery CONN
2nd: 20.F0411.008



S5/Shipping mode



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Title
45_BATT CONN

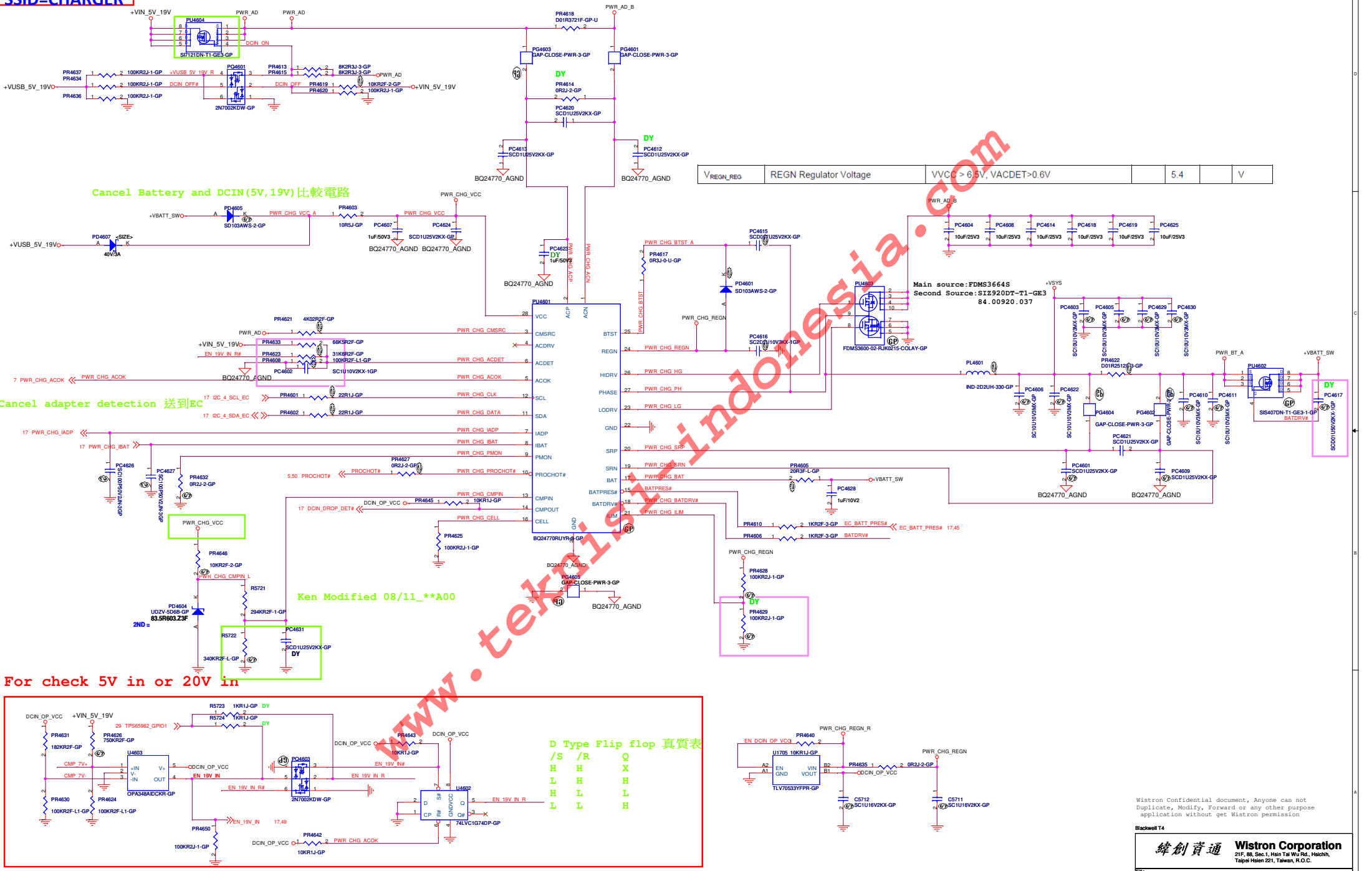
Size Document Number
Blackwell T4

Rev
-1

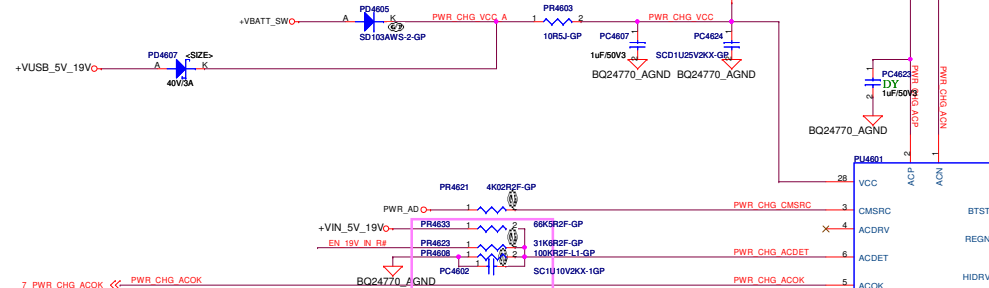
Date: Thursday, October 01, 2015 Sheet 45 of 73

Charger

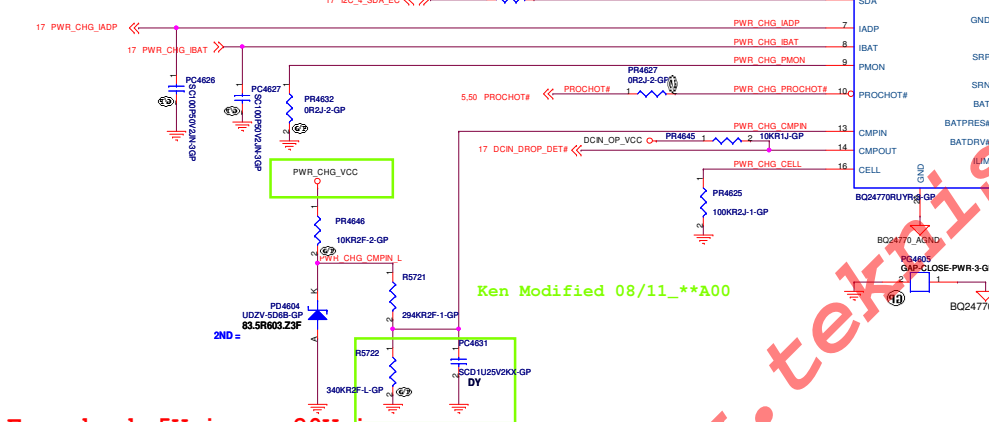
SSID=CHARGER



Cancel Battery and DCIN(5V,19V) 比較電路

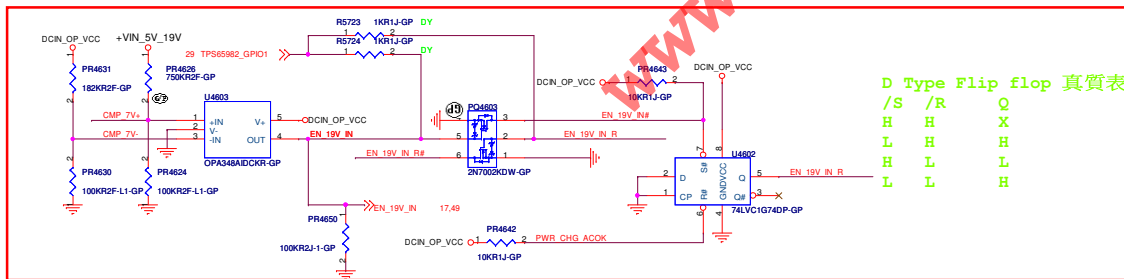


Cancel adapter detection 送到EC



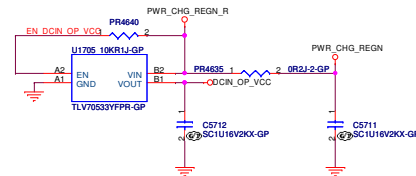
Ken Modified 08/11_**A00

For check 5V in or 20V in



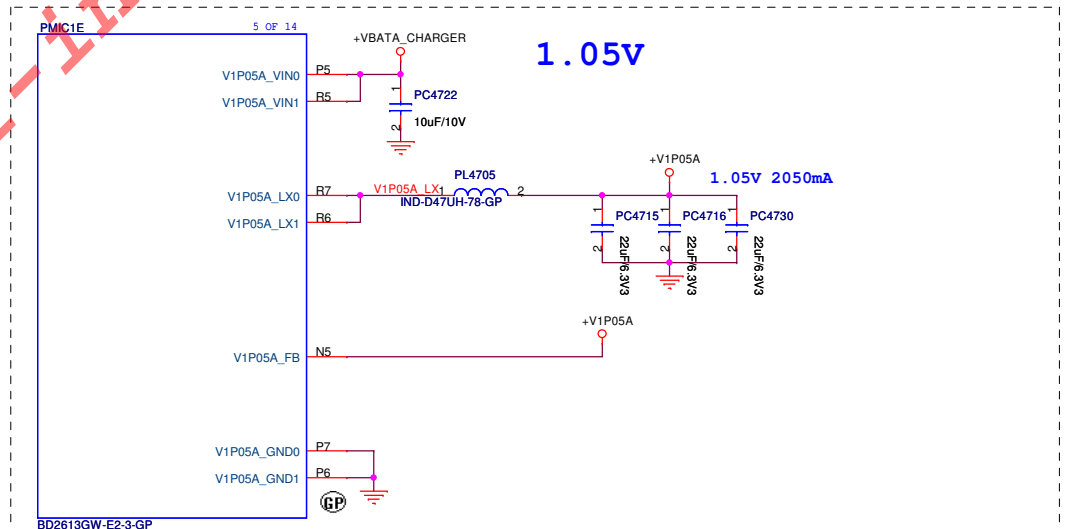
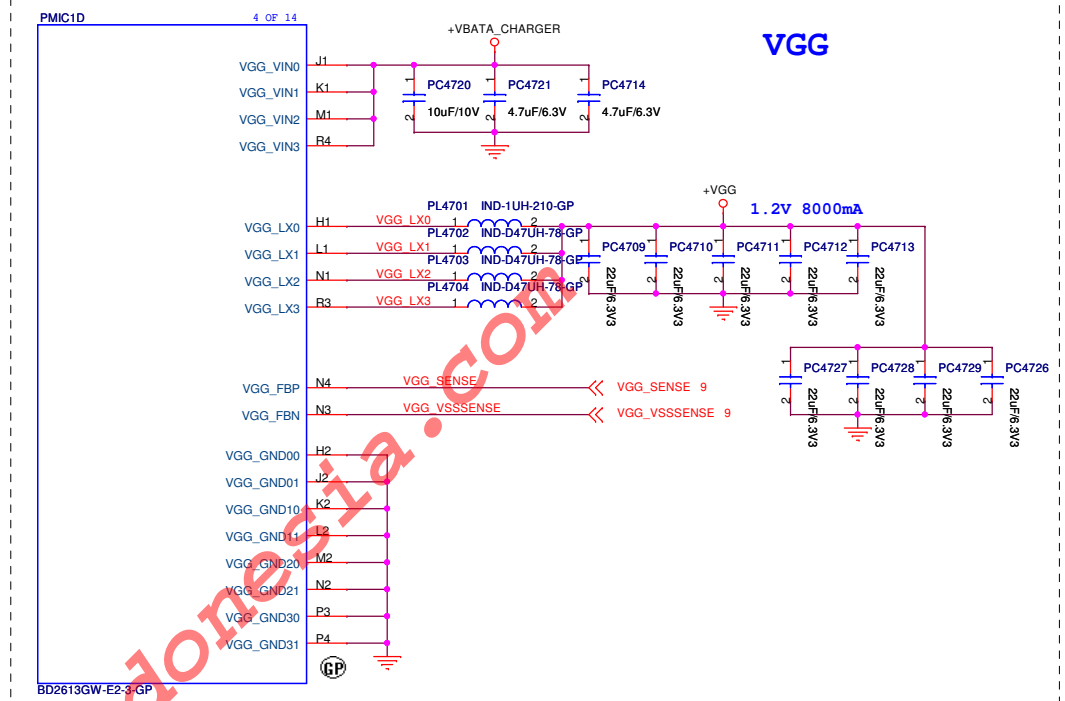
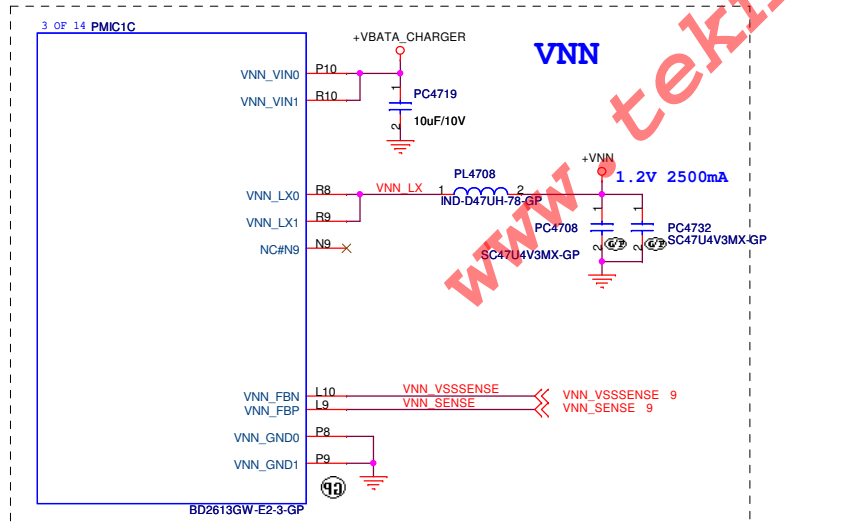
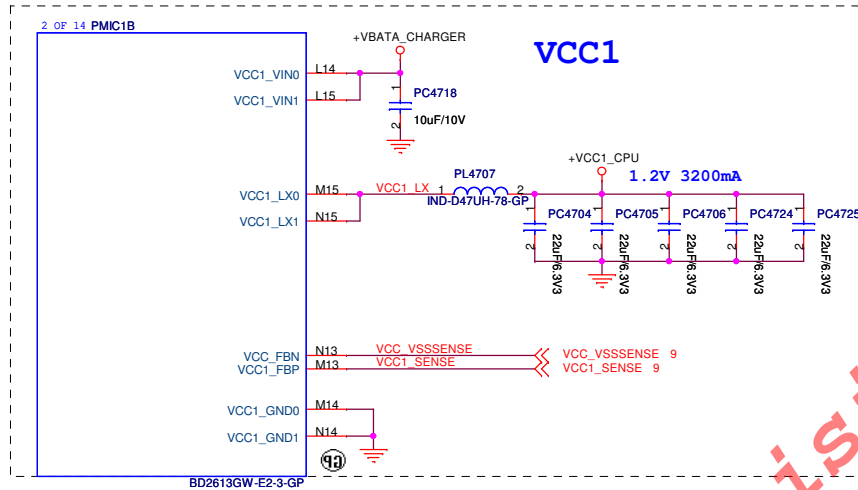
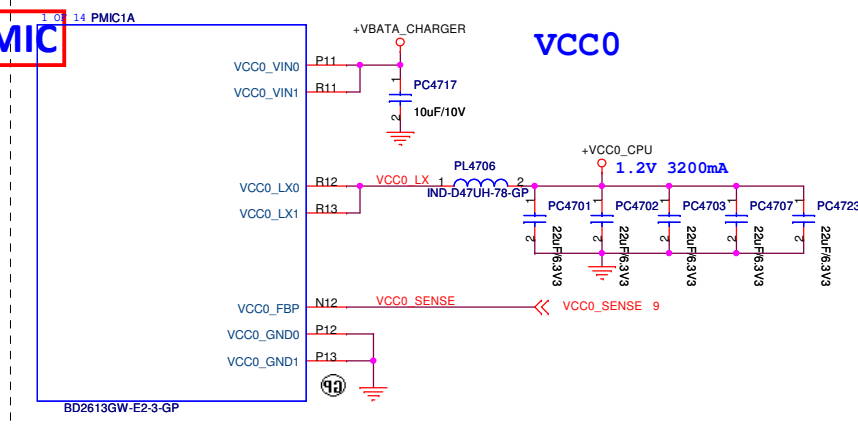
D Type Flip flop 真實表

| /S | /R | Q |
|----|----|---|
| H | H | X |
| L | H | H |
| H | L | L |
| L | L | H |



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SSID=PMIC

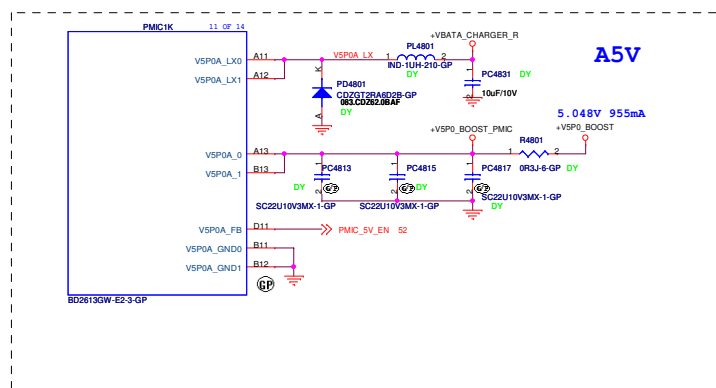
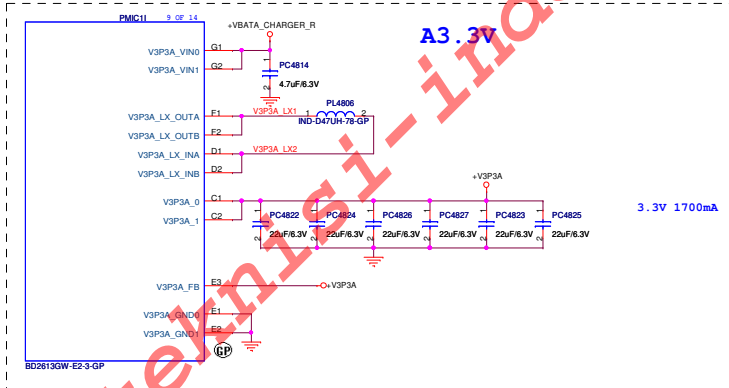
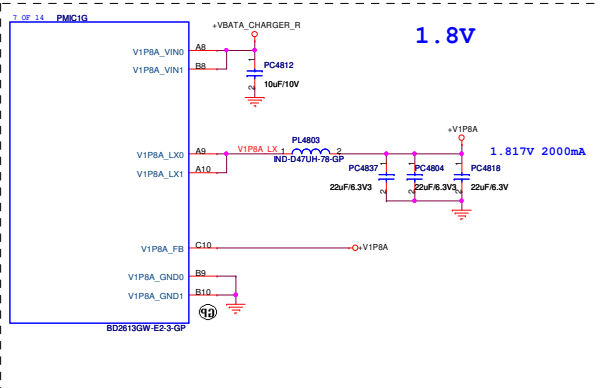
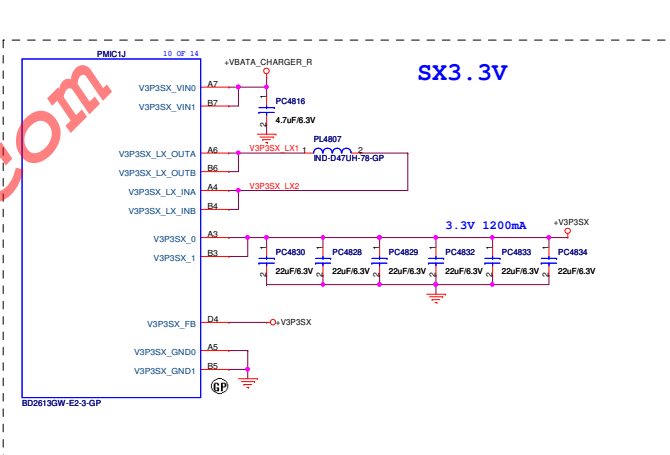
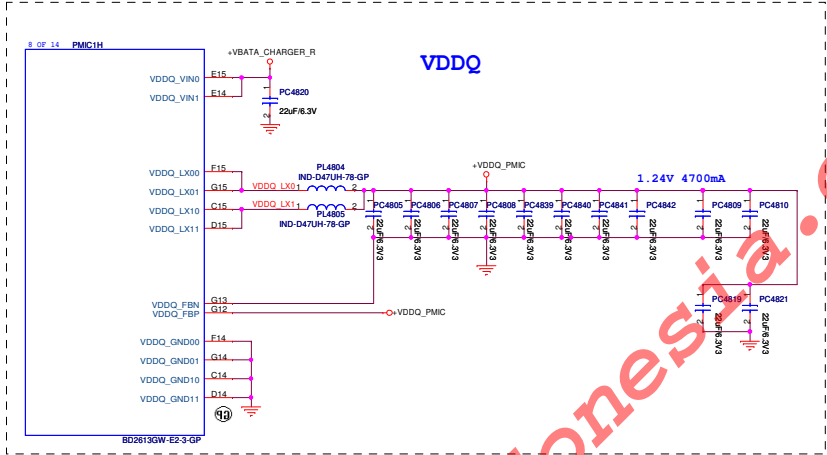
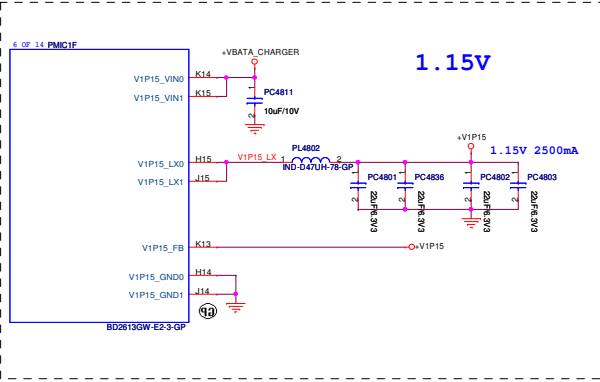


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| <p>Title: 47 PMIC(1/5) (BD2613)</p> | |
| Size | Document Number |
| <p>Blackwell T4</p> | |
| Date: Thursday, October 01, 2015 | Sheet 47 of 73 |
| Rev | -1 |

SSID=PMIC



Rohm PMIC decoupling amount target

| | A1 Stepping | B0 Stepping |
|--------|-------------|-------------|
| VCC0 | 5*47uF | 3*47uF |
| VCC1 | 5*47uF | 3*47uF |
| VNN | 4*47uF | 2*47uF |
| VGG | 4*47uF | 4*47uF |
| VGG | 6*22uF | 4*22uF |
| V1P05A | 4*47uF | 1*47uF |
| V1P15 | 4*47uF | 2*47uF |
| V1P8A | 5*22uF | 3*22uF |
| VDDQ | 8*47uF | 6*47uF |
| V3P3A | 10*47uF | 4*47uF |
| V3P3SX | 8*47uF | 4*47uF |
| V5P0A | 6*10uF | 6*10uF |

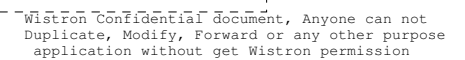
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File 48 PMIC(2/5) (BD2613)
Size Document Number Blackwell T4 Rev -1
Date: Thursday, October 01, 2015 Sheet 48 of 73

SSID=PMIC

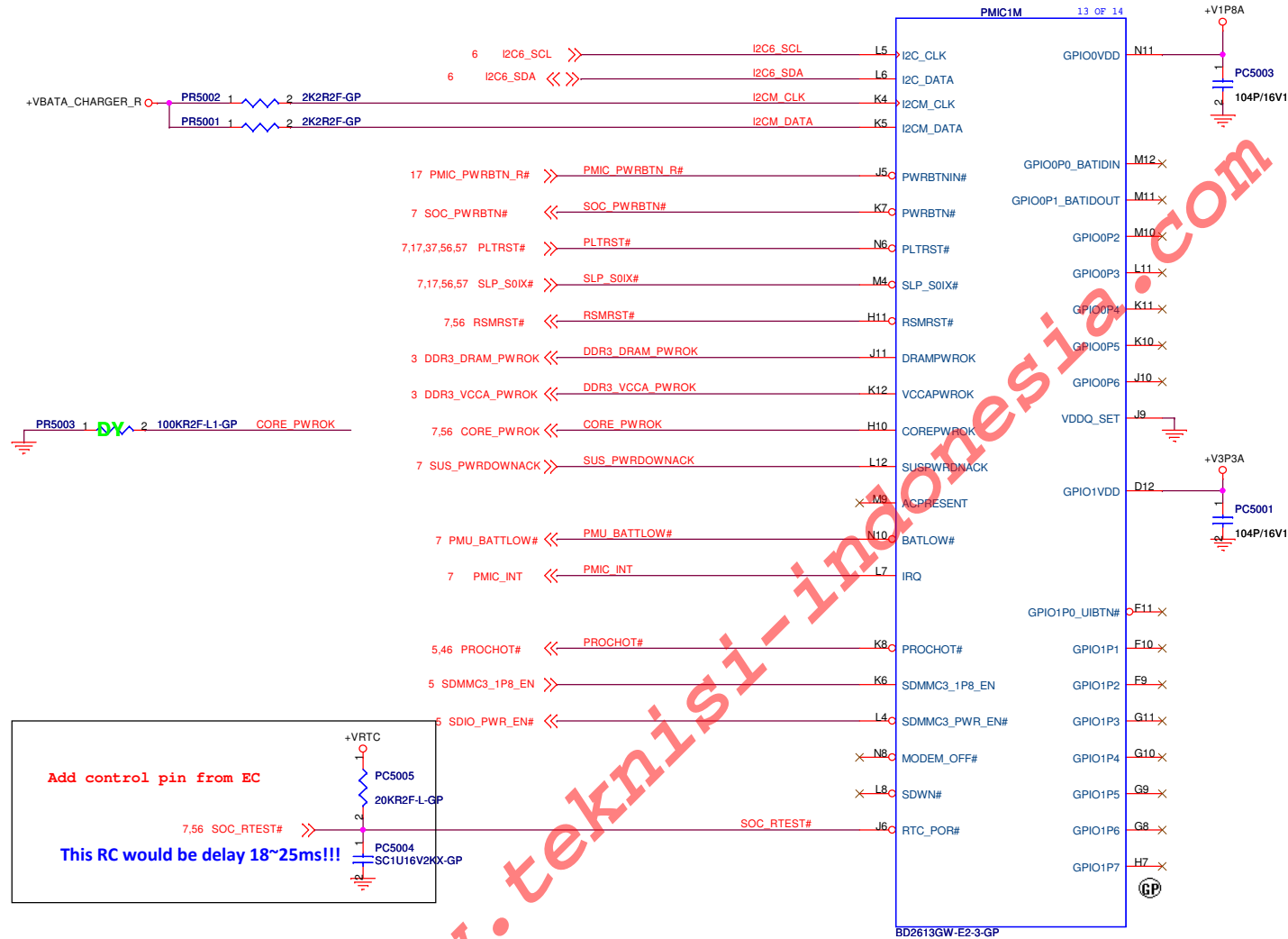


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| | | | |
|-----------------------|----------------------------|-------------|-----|
| Title | | | |
| 49 PMIC(3/5) (BD2613) | | | |
| Size | Document Number | | Rev |
| | Blackwell T4 | | -1 |
| Date: | Thursday, October 01, 2015 | Sheet 49 of | 73 |

SSID=PMIC



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| | | | |
|----------------------------------|--|-----------------------|--|
| Title | | 50 PMIC(4/5) (BD2613) | |
| Size | | Document Number | |
| Date: Thursday, October 01, 2015 | | Sheet 50 of 73 | |
| Blackwell T4 | | Rev -1 | |

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SSID=PMIC

Check location and value

Analog GND

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<Core Design>

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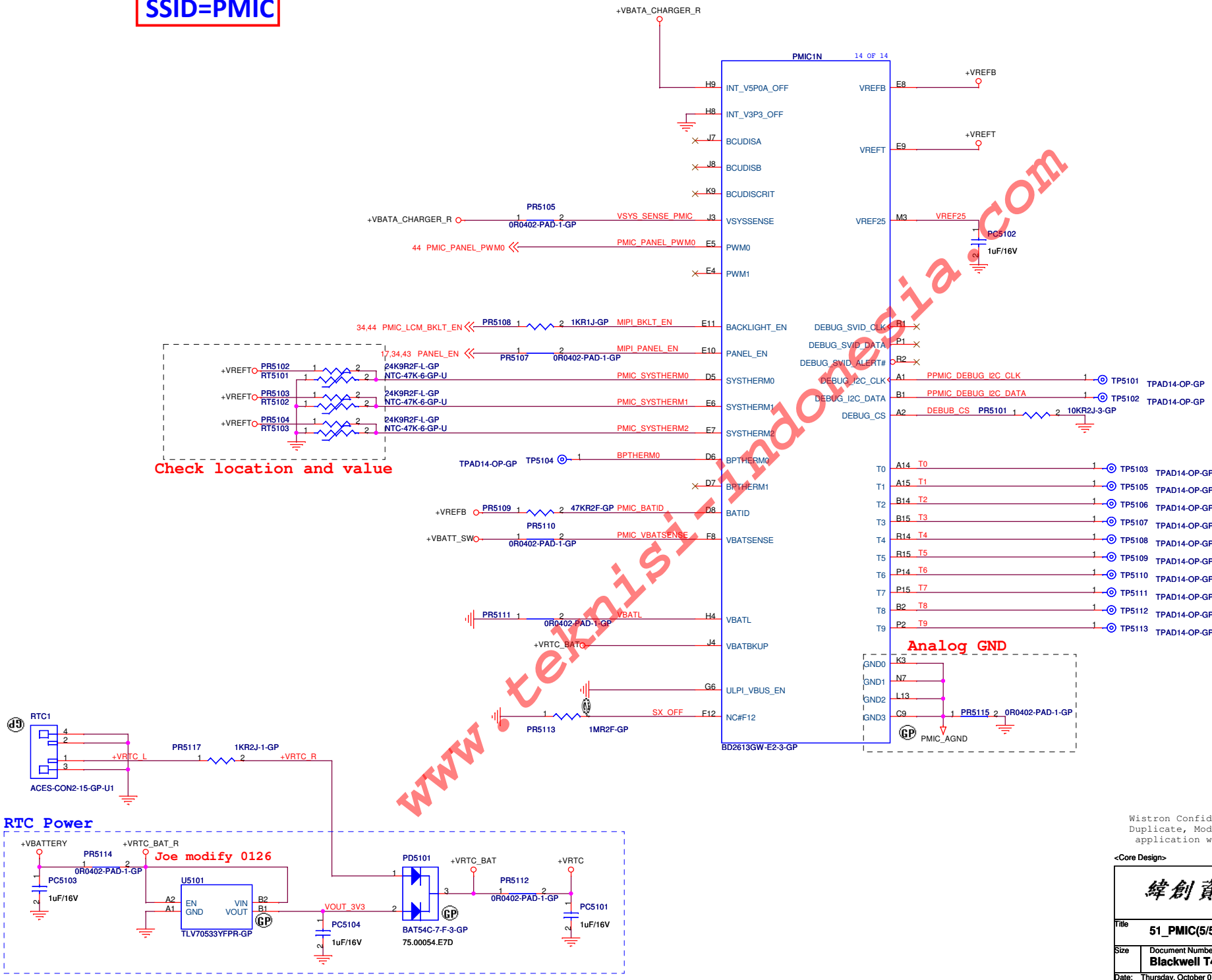
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Size Document Number
Blackwell T4

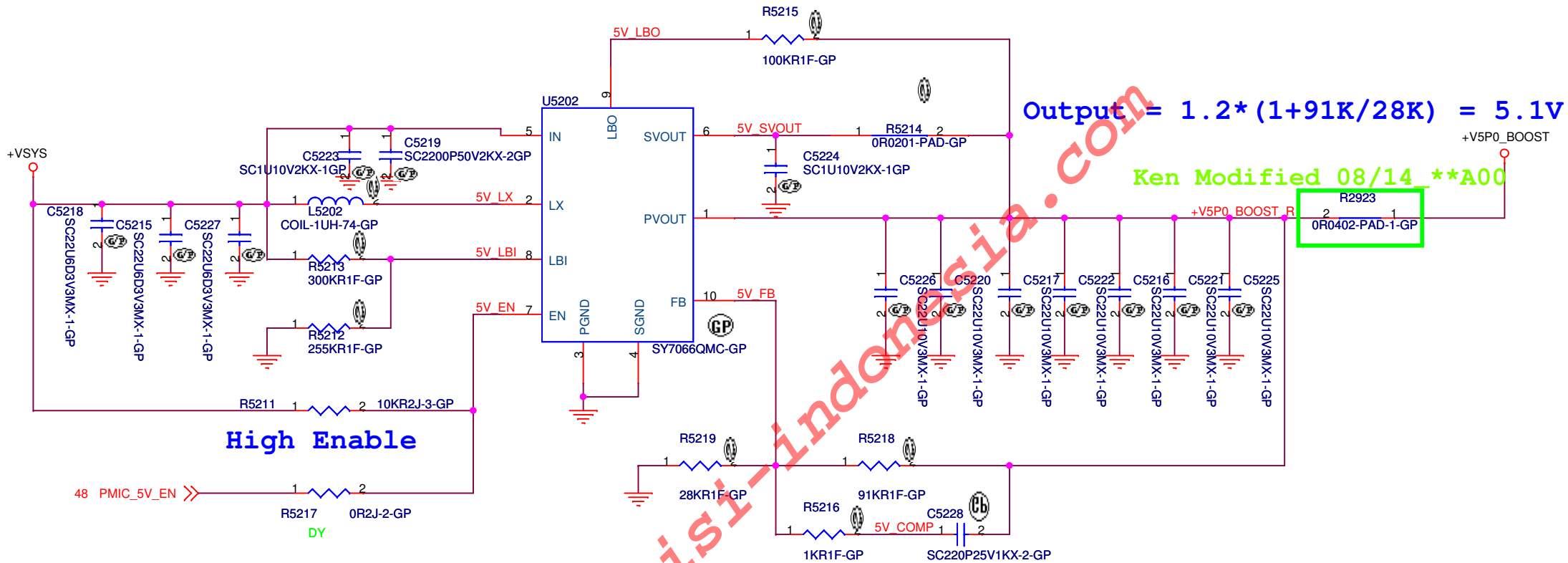
Date: Thursday, October 01, 2015

Sheet 51 of 73

Rev
-1



SSID=PWR.Plane.Regulator_5v



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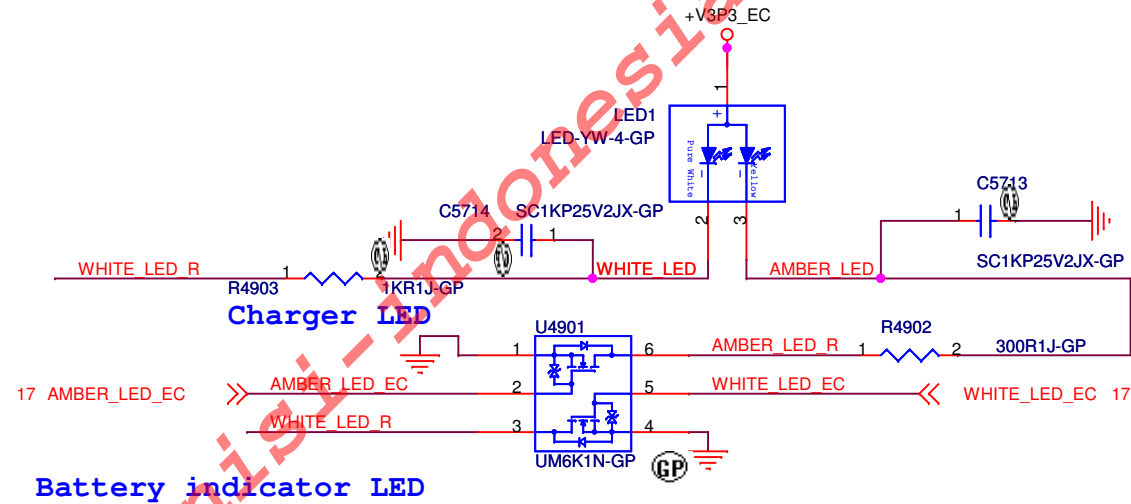
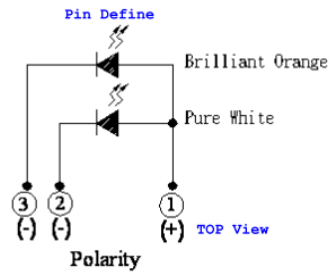
Title **52_5V_BOOST & 3.3V(Reserved)**

| | | |
|------|---------------------|-----------|
| Size | Document Number | Rev |
| | Blackwell T4 | -1 |

Date: Thursday, October 01, 2015 Sheet 52 of 73

POWER/Charger LED

SSID=User.Interface



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Title
53_POWER LED/DOCK CONN

Size
Document Number
Blackwell T4

Rev
-1

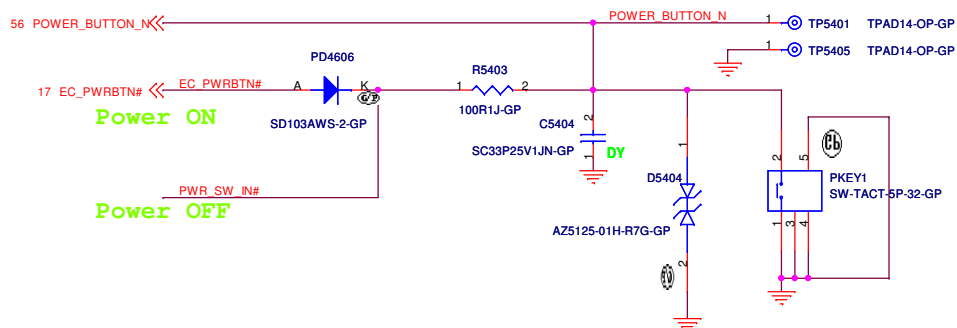
Date: Thursday, October 01, 2015

Sheet 53 of 73

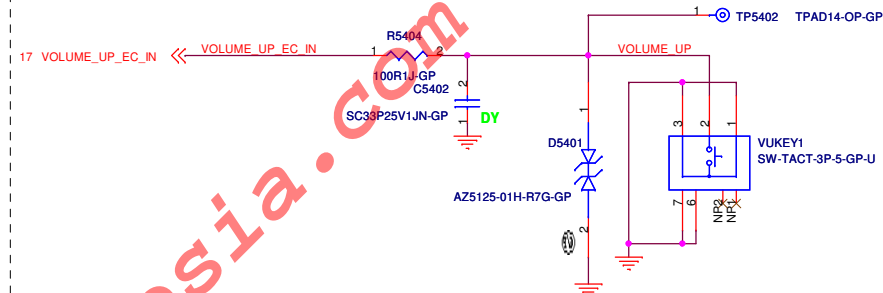
PWR Button / Volum Key / Home key

SSID=User.Interface

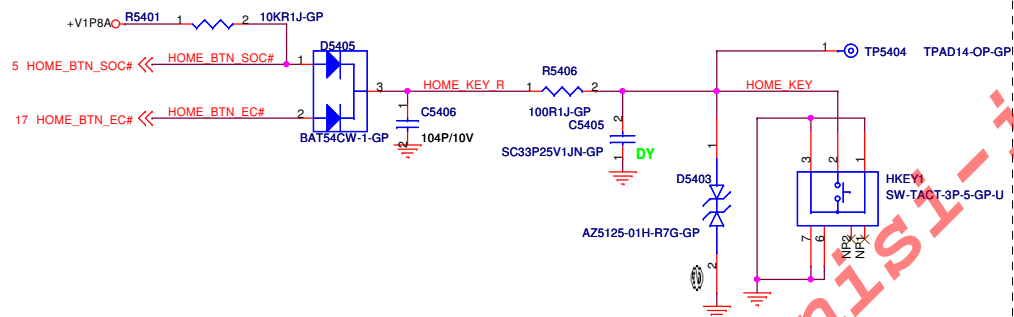
POWER KEY



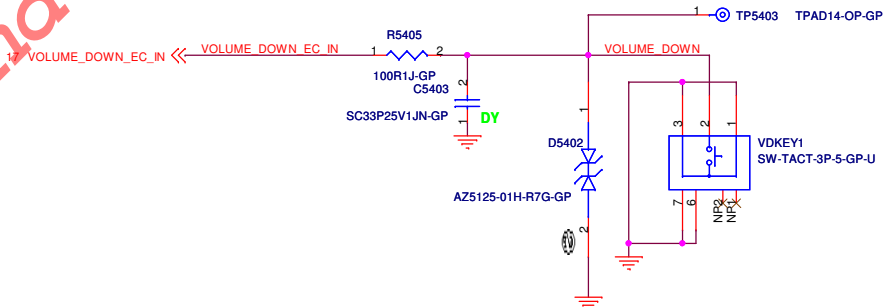
VOLUME UP KEY



HOME KEY



VOLUME DOWN KEY

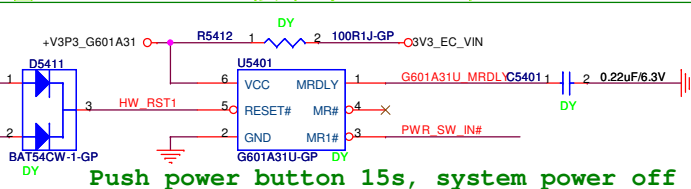


SYSTEM POWER ON

EC latch System power on



當Power Butoton 按下時,Reset#為LOW,Power Button 放開時,Reset#為Hgh.



Push power button 15s, system power off

當長按16S, System Power off

$$T=76000 \times 0.22\mu F = 16.72ms$$

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| | | |
|----------------------------------|------------------------------|--------|
| Title 54_PWR/Volume/Home Button | | |
| Size | Document Number Blackwell T4 | Rev -1 |
| Date: Thursday, October 01, 2015 | Sheet 54 of 73 | |

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Title

55_IO Board Connector(Reserved)

Size

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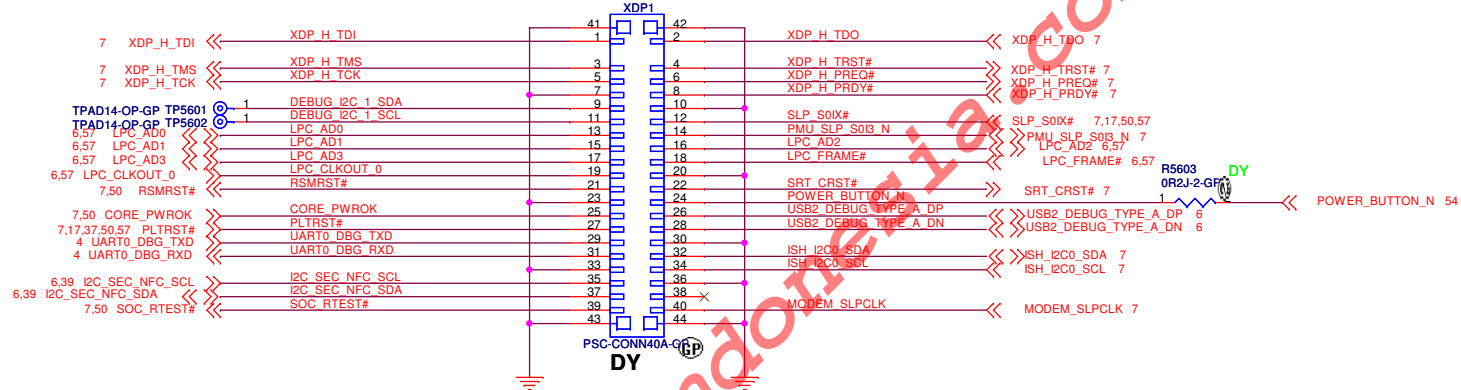
Date: Thursday, October 01, 2015

Sheet 55 of 73

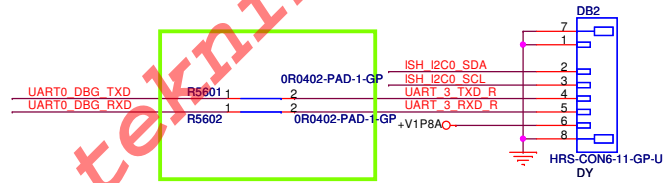
XDP Debug Connector

SSID=XDP

Debug Connector with XDP



SW Debug Connector



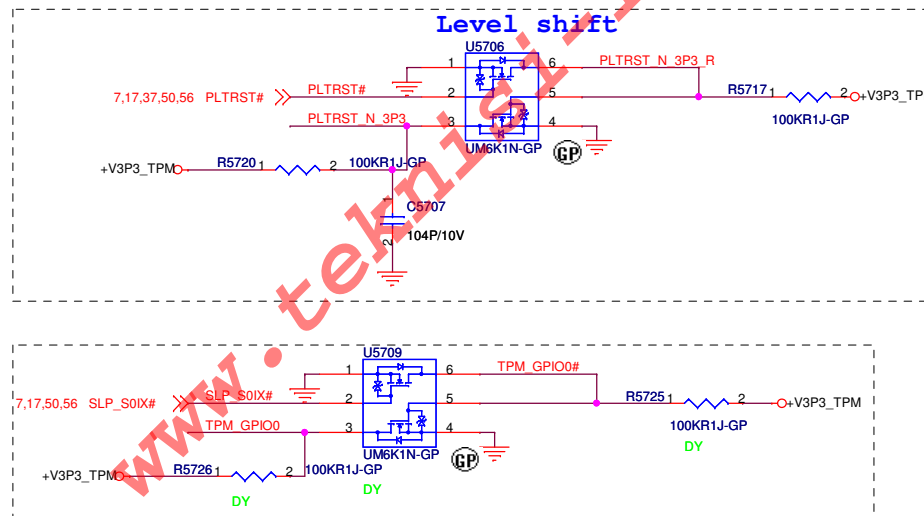
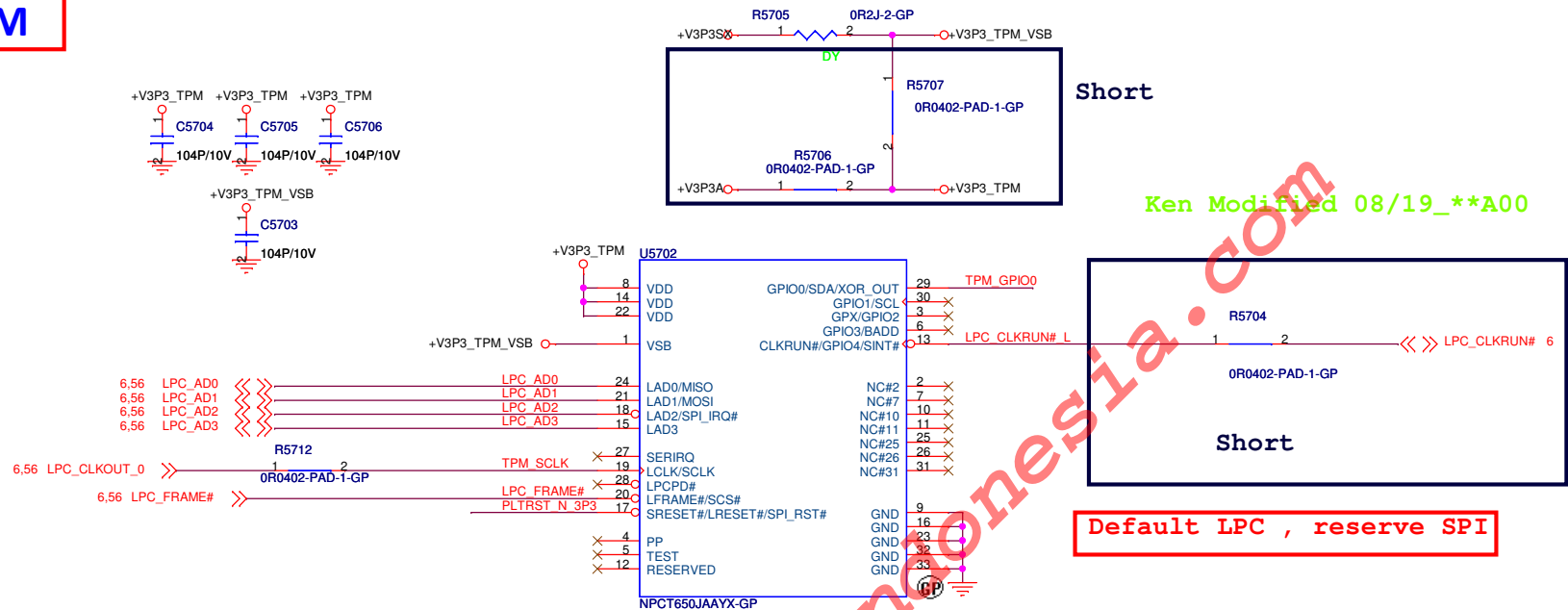
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|---|------------------------------|--------|
| Title 56_XDP Connector | | |
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SSID=TPM



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|-------|----------------------------|-------|----------|
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| | Blackwell T4 | -1 | |
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Title

58_Docking Connector(Reserved)

Size

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Date: Thursday, October 01, 2015

Sheet 58 of 73

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Title

59_CPU_XDP(Reserved)

Size

Document Number

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Rev

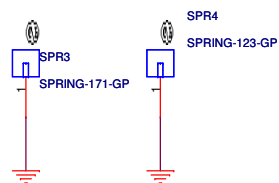
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Date: Thursday, October 01, 2015

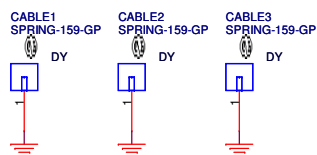
Sheet 59 of 73

Shielding Can

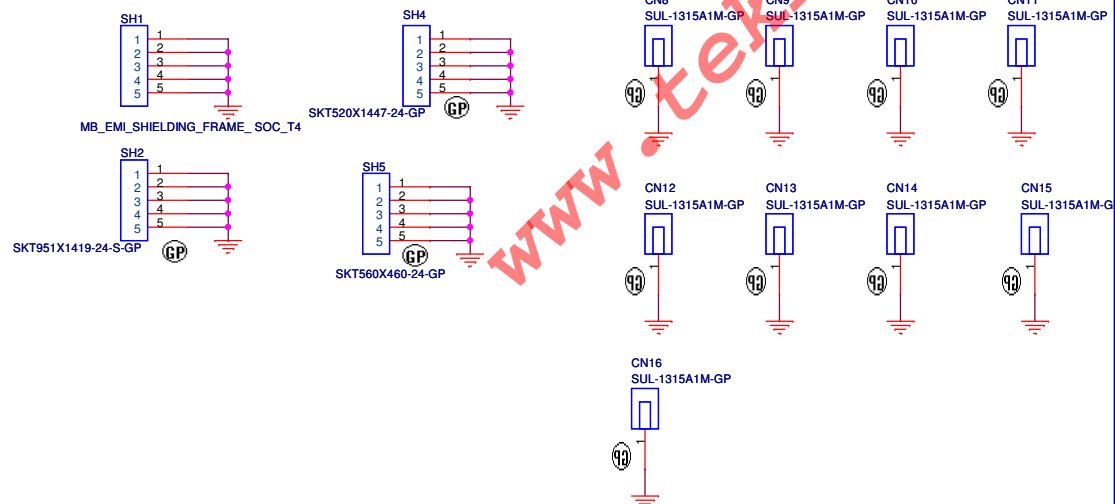
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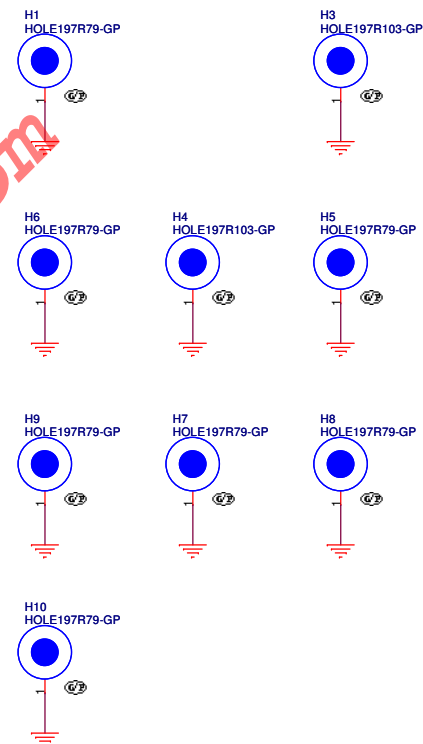
Joe modify 0114



Joe modify 0114



Screw Hole



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| Title | | |
| 60_ME/EMI | | |
| Size | Document Number | Rev |
| | Blackwell T4 | -1 |
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| Sheet 60 of 73 | | |

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Title

61_RF(Reserved)

Size

Document Number

Blackwell T4

Rev

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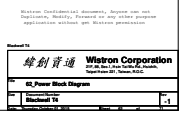
Date: Thursday, October 01, 2015

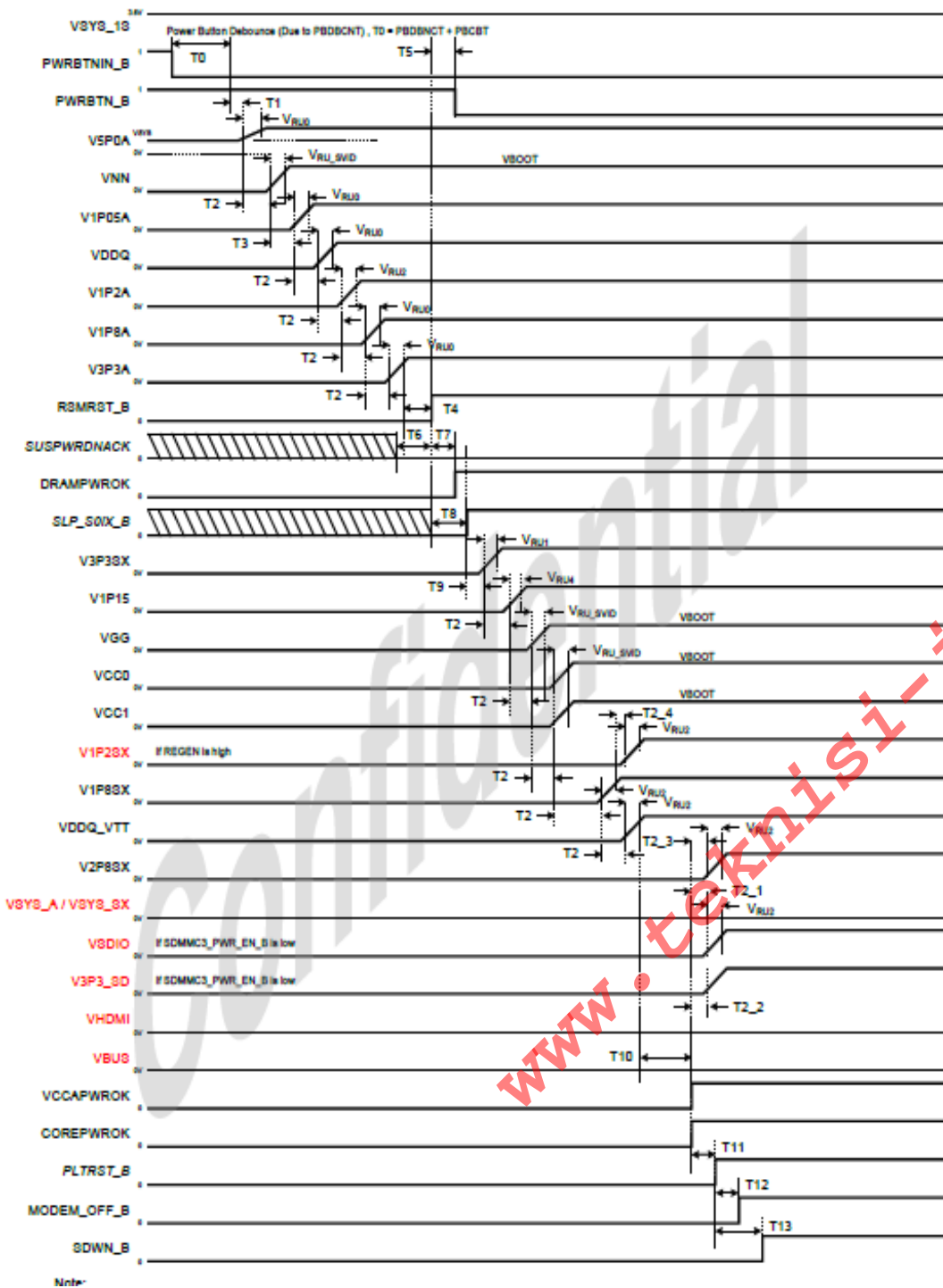
Sheet 61 of 73

The diagram illustrates the internal architecture of the TP65982 USB Type C Controller and Charger IC. It shows the following components and their connections:

- Input/Output:**
 - DCIN detect** and **VBUS detect** inputs.
 - Charger BQ24770** and **TP65982** blocks.
- Regulators:**
 - Buck-Boost Regulator1** (rating: 1700mA)
 - Buck-Boost Regulator2** (rating: 1900mA)
 - Boost Regulator** (rating: 950mA)
 - Power Switch**
 - Linear Regulator** (rating: 325mA)
- Sensors and Control Blocks:**
 - SAR Sensor (EX9500ULTXT)**
 - Gyro Sensor (LSG200TRA)**
 - G Sensor + S-Compass (LSM303CTR)**
 - Touch Panel**
 - TPM (NCT655JAAIX)**
 - USB Type C Controller (TP65982)**
 - Charger (BQ24770)**
- Other Components:**
 - DCIN detect** and **VBUS detect** inputs.
 - TP65982** and **Charger BQ24770** blocks.

The diagram is labeled with "www.teknisi-indonesia.com" and "www.teknisi-indonesia.com".



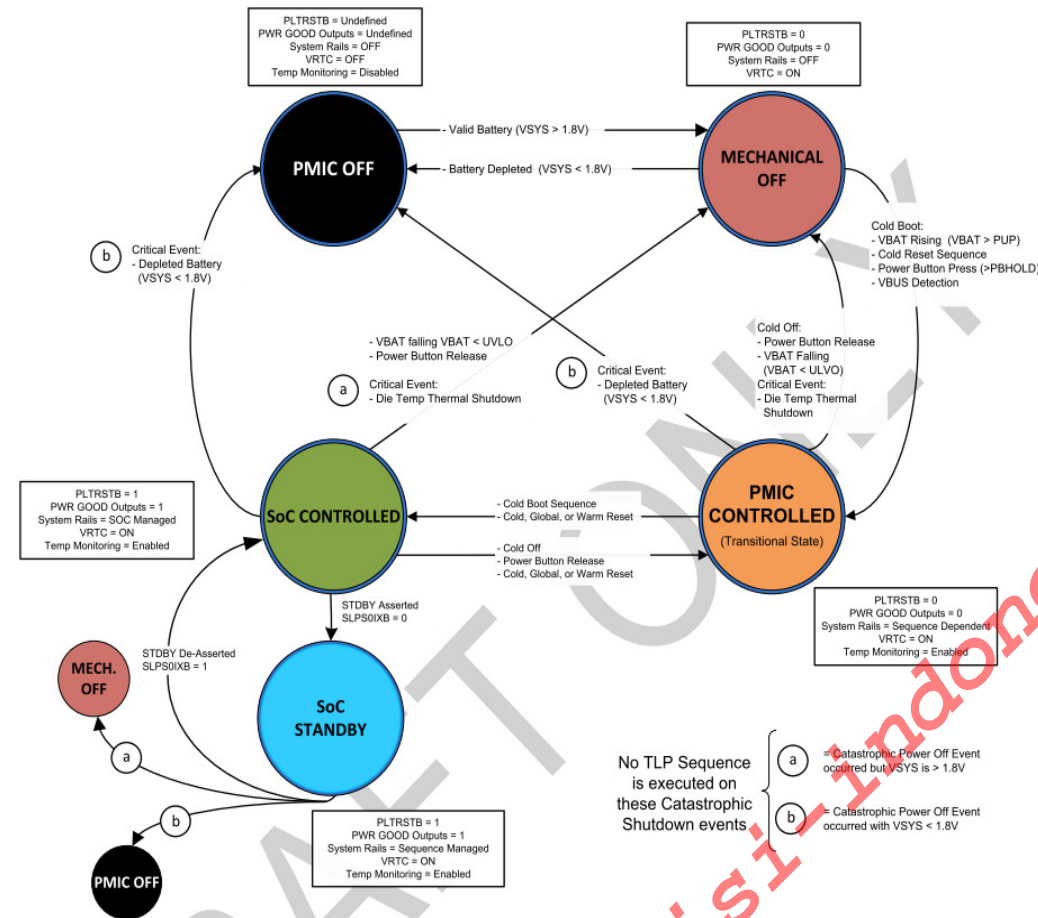


| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------|---|--------------|---------|--------------|------|
| T0 | Power Button Debounce Time (Due to PBDBNCT register) | PBDBNCT -10% | PBDBNCT | PBDBNCT +10% | ms |
| T1 | After battery detect or power button debounce time to VSP0A turn on delay | 0 | 24 | 500 | µs |
| T2 | Rail to subsequent rail turn-on delay for all rails unless specified otherwise | 0.01 | 1 | 2 | ms |
| T2_1 | COREPWROK assertion (high) to VSDIO turn on (10%) delay | 10 | 50 | 100 | µs |
| T2_2 | COREPWROK assertion (high) to V3P3_SD turn on (10%) delay | 0.1 | 0.45 | 1 | ms |
| T2_3 | COREPWROK assertion (high) to V2P8SX turn on (10%) delay | 0 | 10 | 50 | µs |
| T2_4 | V1P8SX Valid (90%) to V1P2SX turn on (10%) delay | 0 | 30 | 60 | µs |
| T3 | VNN to V1P05A turn on delay (CCB 034 from Intel) | 0.5 | 1 | 2 | ms |
| T4 | V3P3A valid (90% level) to RSMRST_B de-assertion (high) if SUSPWRDNACK is low | 0 | 24 | 500 | µs |
| T5 | RSMRST_B de-assertion (high) to the instant when the BD2613GW outputs a level shifted copy of PWRBTN_B, i.e. PWRBTN_B | 0 | 24 | 32 | µs |
| T6 | SUSPWRDNACK de-assertion (low) to RSMRST_B de-assertion (high) | 0 | - | - | µs |
| T7 | RSMRST_B de-assertion (low) to DRAMPWROK assertion (high) | 0 | 24 | 32 | µs |
| T8 | RSMRST_B de-assertion (high) to SLP_S0IX_B de-assertion (high) | 20 | - | - | µs |
| T9 | SLP_S0IX_B de-assertion (high) to V3P3SX start to turn on (10% output voltage level) delay | 0 | 250 | 500 | µs |
| T10 | Core rails valid to VCCAPWROK and COREPWROK assertion (high) | DTPWROK -20% | DTPWROK | DTPWROK +20% | ms |
| T11 | COREPWROK assertion (high) to PLTRST_B de-assertion (high) | 60 | - | - | µs |
| T12 | MODEM_OFF_B de-assertion (high) delay from PLTRST_B de-assertion (high) | 10 | 20 | 40 | µs |
| T13 | SDWN_B de-assertion (high) delay from PLTRST_B de-assertion (high) | 40 | 60 | 75 | µs |

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| Title 64_Power Sequence Timing | |
| Size Document Number Blackwell T4 | Rev -1 |
| Date: Thursday, October 01, 2015 Sheet 64 of 71 | |



| | PART | BUCK1 | BUCK2 | BUCK3 | BUCK4 | BUCK5 | BUCK6 | LD01 | LD02 | LD03 | LD04 | VREFDQ | LD05 | LD06 | LD07 | LD08 | LD09 | LD010 | LD011 | LD012 | LD013 | LD014 | Comment |
|-----------------|------|-------|-------|-------|-------|-------|-------|------|------|------|------|--------|------|------|------|------|------|-------|-------|-------|-------|-------|--|
| PMIC OFF | BYT | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| | CHT | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| Mechanical Off | BYT | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| | CHT | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | ON | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | |
| SoC Control led | BYT | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | Disabled by default. SoC can enable/disable according to system activity |
| | CHT | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | Disabled by default. SoC can enable/disable according to system activity |
| SoC Stand-by | BYT | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | OFF | Will keep whatever state had before entering standby |
| | CHT | OFF | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | ON | Will keep whatever state had before entering standby |

LDO7-LDO14 will keep whatever state before entering standby, it's up to the user whether to enable/disable. State machine won't enforce the behavior in this case.

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Title **65_Power State**

Size Document Number **Blackwell T4**

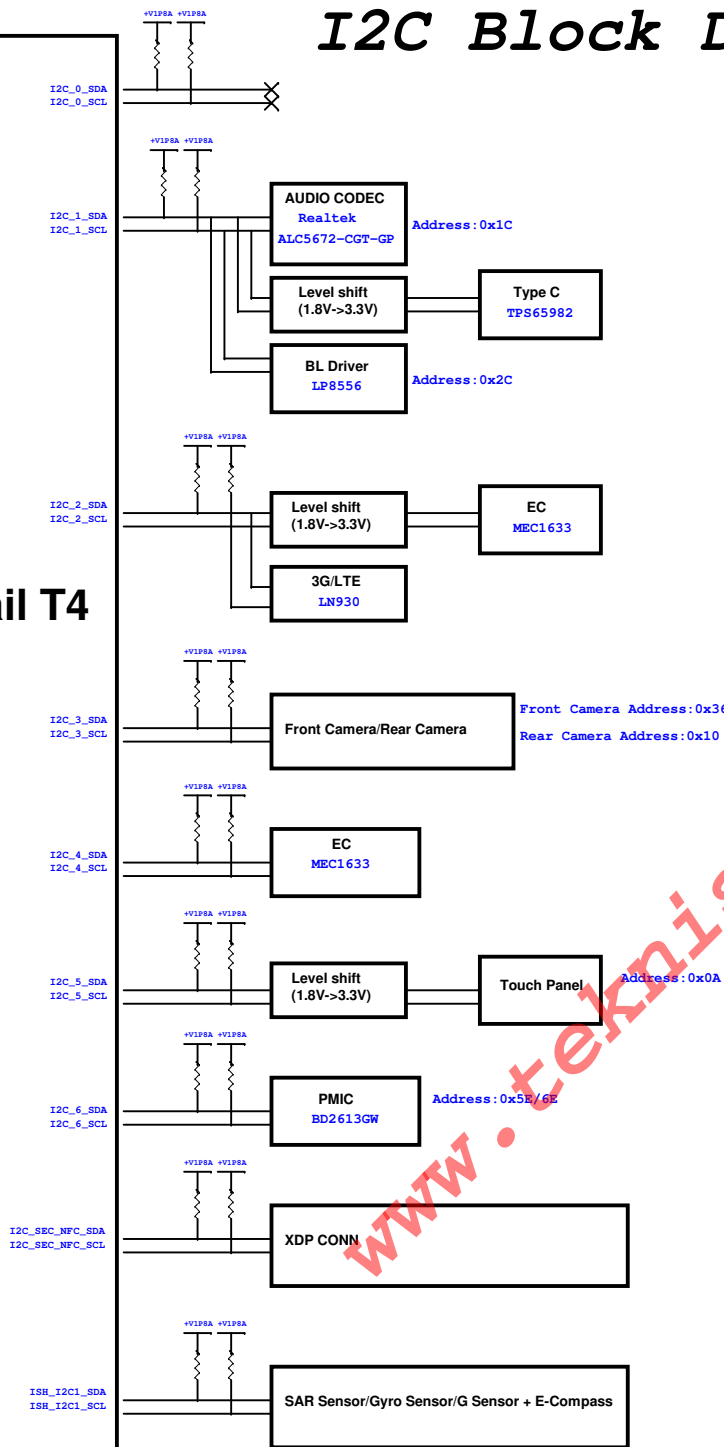
Date: Thursday, October 01, 2015

Sheet 65 of 73

Rev -1

I2C Block Diagram

Intel Cherry Trail T4



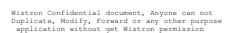
| Device | Blackwell-T3 | Blackwell-T4 | Somerset-T4 |
|-------------------------------|--------------|--------------|--------------|
| CODEC | I2C1 | I2C1 | I2C1 |
| AMP | --- | --- | I2C1 |
| Type C PD controller | I2C1/EC I2C7 | I2C1/EC_I2C7 | I2C1/EC_I2C7 |
| 3G/LTE | I2C1 | I2C2 | I2C2 |
| EC (I2C_0) | I2C2 | I2C2 | I2C2 |
| Front CAMERA | I2C2 | I2C3 | I2C3 |
| Rear CAMERA | I2C2 | I2C3 | I2C3 |
| ISP | I2C2 | I2C3 | I2C3 |
| uHDMI | --- | --- | DDIO_DDC |
| NFC | I2C2 | NFC_I2C | NFC_I2C |
| EC (I2C_5) | I2C4 | I2C4 | I2C4 |
| LCD Backlight Driver | I2C1 | I2C1 | --- |
| Touch | I2C5 | I2C5 | I2C5 |
| PMIC | I2C6 | I2C6 | I2C6 |
| A+Gyro sensor/ Gyro sensor | ISH_I2C | ISH_I2C | ISH_I2C |
| E sensor/ E+A sensor | ISH_I2C | ISH_I2C | ISH_I2C |
| Sar Sensor | ISH_I2C | ISH_I2C | ISH_I2C |
| Battery | EC_SMB3 | EC_SMB3 | EC_SMB3 |
| Charger | EC_I2C4 | EC_I2C4 | EC_I2C4 |

The schematic diagram illustrates the SoC interface connections. On the left, the SoC pins are grouped into several sections:

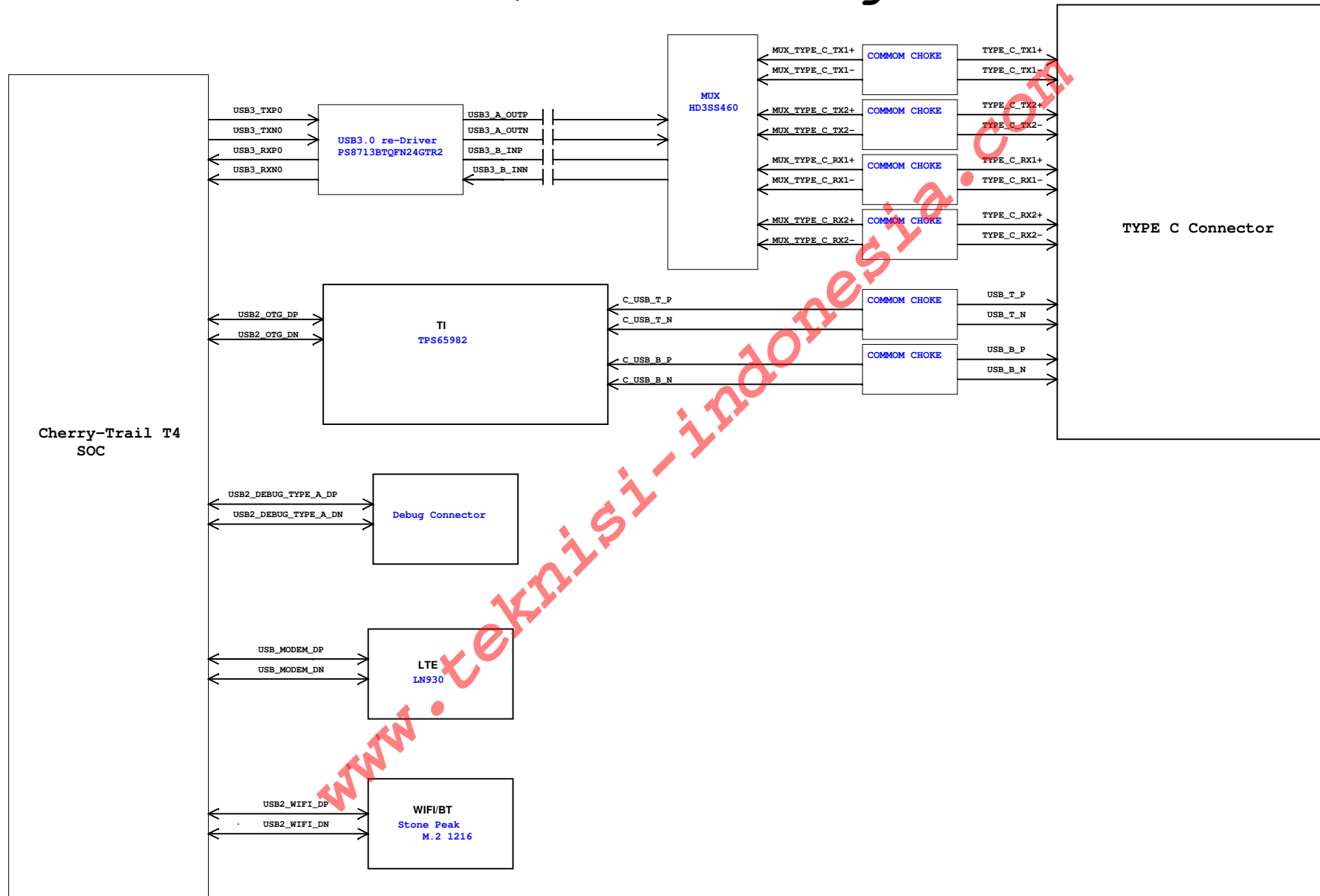
- MC12_2 Data and Control:** MC12_2_DATA0_DN, MC12_2_DATA0_DP, MC12_2_DATA1_DN, MC12_2_DATA1_DP, MC12_2_CLK_DN, MC12_2_CLK_DP.
- MC12_1 Data and Control:** MC12_1_DATA0_DN, MC12_1_DATA0_DP, MC12_1_DATA1_DN, MC12_1_DATA1_DP, MC12_1_CLK_DN, MC12_1_CLK_DP.
- RTC Section:** RTC_XTAL_IN, RTC_XTAL_OUT, RTC_X1, RTC_X2.
- CLK_T2S_MCLK:** CLK_T2S_MCLK.
- MC12_C Data and Control:** MC12_C_CLK_DN, MC12_C_CLK_DP.
- EMMC_CLK:** EMMC_CLK.

 The SoC pins are connected to various external components:

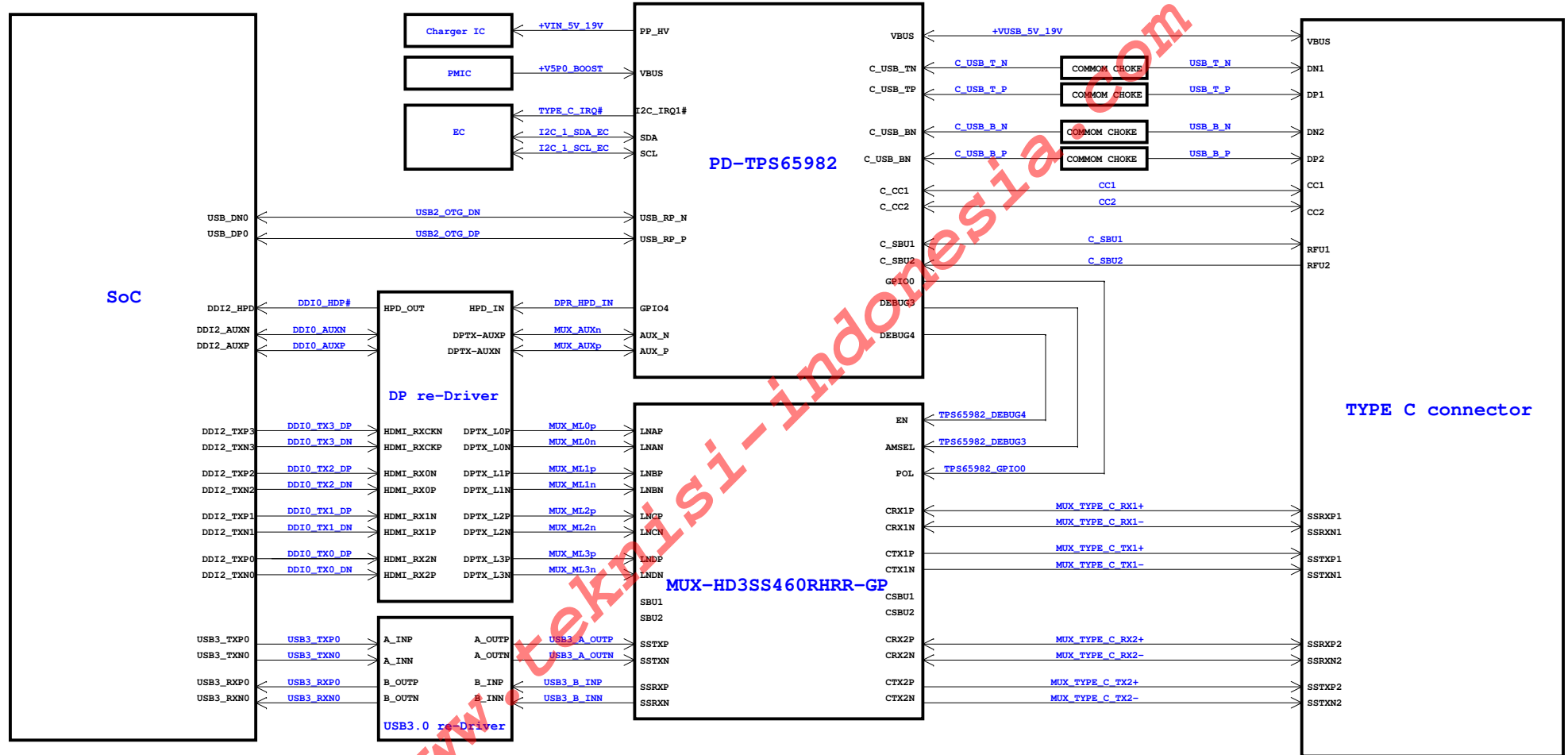
- PCIE Section:** PCIE_REFCLK0_P, PCIE_REFCLK0_N, PCIE_CLKREQ0_N, PCIE_CLKP0, PCIE_CLKN0, PCIE_CLKREQ0#.
- 3G/LTE Module:** A 3G/LTE Module (Telit LN930) is connected to the RF_LTE_SIM1_CLK pin.
- SD CARD:** An SD CARD is connected to the SD3_CLK pin.
- LPDDR3 Memory:** Two LPDDR3 memory modules (H9CCNNBKTMLBR-NTD-GP) are connected to the LPDDR3_M0_CLK_DN_A, LPDDR3_M0_CLK_DP_A, LPDDR3_M0_CLK_DN_B, and LPDDR3_M0_CLK_DP_B pins.



USB I/O Block Diagram



TYPE C Block Diagram



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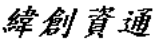
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| Title <div>70_TYPE C BLOCK DIAGRAM(2/2)(Reserved)</div> | | |
| Size | Document Number <div>Blackwell T4</div> | Rev <div>-1</div> |
| Date: Thursday, October 01, 2015 | | Sheet 70 of 73 |

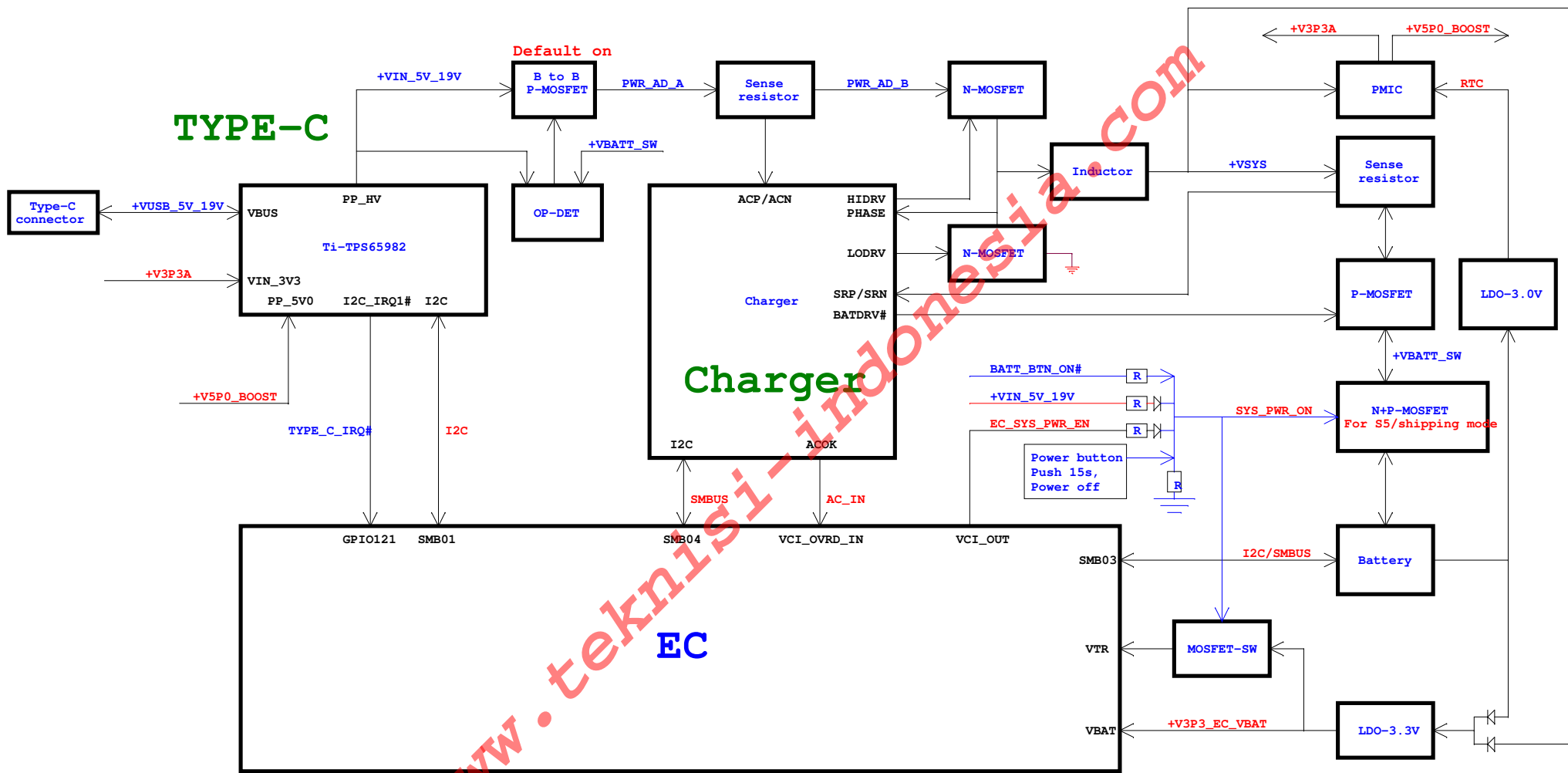
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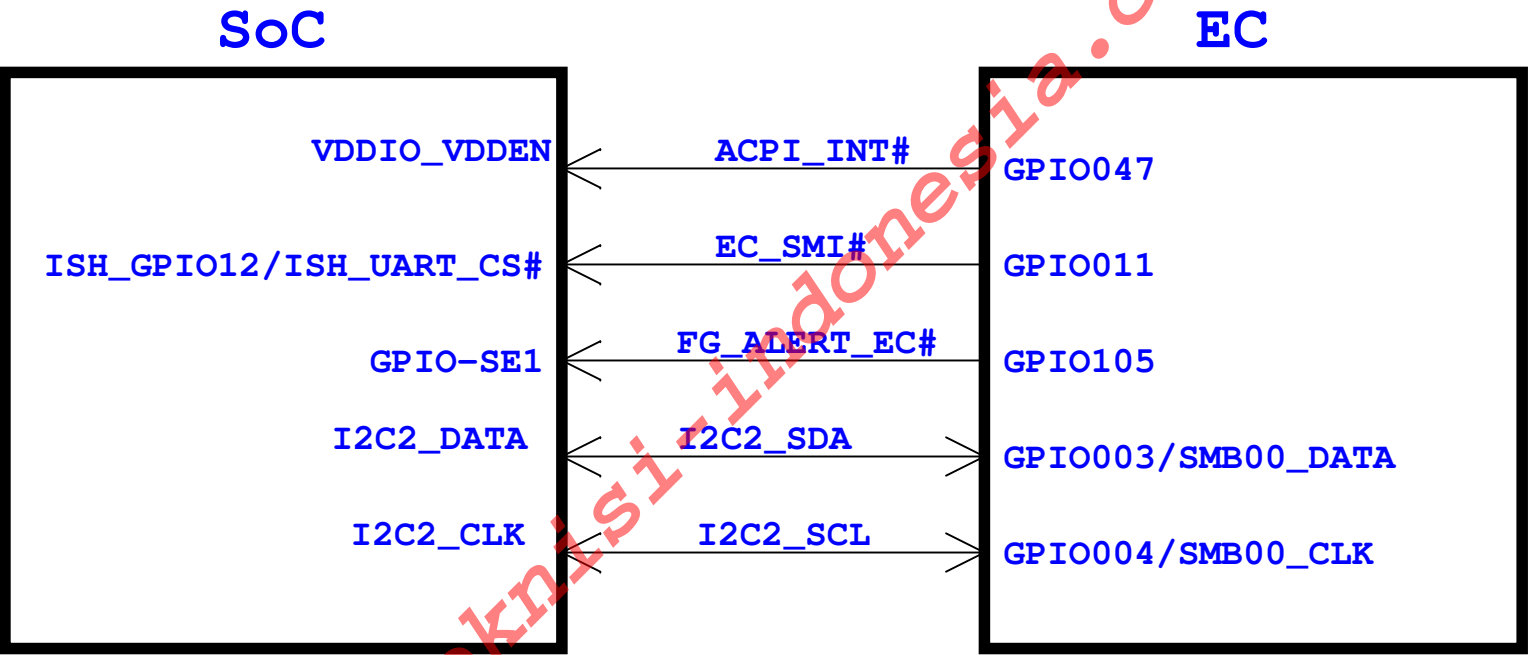
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| Title 71_Change History | | | |
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Power block diagram



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EC/SoC interface



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Title **73_EC/SoC interface**

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